HEWLETT PACKARD

APPLICATION NOTE 944-1

Microwave Transistor Bias Considerations

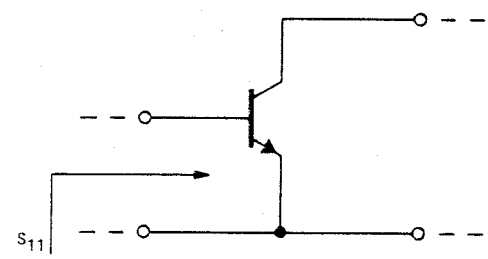
INTRODUCTION

Often the least considered factor in microwave transistor circuit design is the bias network. Considerable effort is spent in measuring s-parameters, calculating gain, and optimizing bandwidth and noise figure, while the same resistor topology is used to bias the transistor. Since the cost per dB of microwave gain or noise figure is so high, the circuit designer cannot afford to sacrifice RF performance by inattention to dc bias considerations.

Microwave transistor amplifier design requires biasing the transistor into the active region of performance and holding this bias or quiescent point constant over variations in temperature. At low frequencies, emitter resistor stabilization with negative current feedback is used for dc stability. At microwave frequencies the bypass capacitor becomes a problem since a good RF bypass at the design frequency often introduces low frequency instability and gives rise to bias oscillations. Figure 1 shows this effect.

In low noise amplifier applications, even if a capacitor could be chosen to provide effective RF *and* low frequency emitter bypass, any small series emitter impedance at the operating frequency would reflect in a large noise figure degradation. Most microwave circuit designs for best gain or lowest noise figure will require that the emitter lead be dc grounded as close to the package as possible so that the emitter series feedback is kept at an absolute minimum.

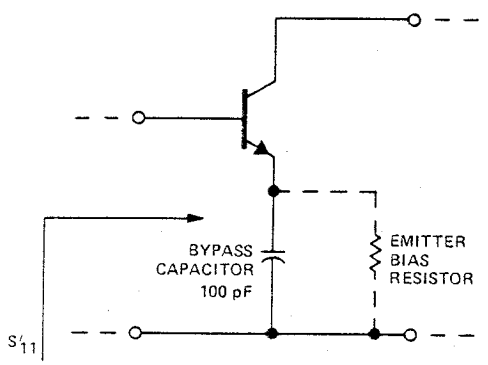
It has been found* that the principle dependent variable in dc stability analysis is the collector current (I_C). The transistor parameters that are temperature sensitive and influence I_C are examined along with some passive resistive circuits that give stable dc operation and allow for trimming due to variations in transistor types.



S_{11} (at 4 GHz) = .52 ∠154°

S_{11} (at .1 GHz) = .901 ∠−14.9°

s-parameters of grounded emitter transistor at 4 GHz and .1 GHz.



S'_{11} (at 4 GHz) = .52 ∠154° unchanged at 4 GHz

S'_{11} (at .1 GHz) = 1.066 ∠−8.5° $|S_{11}|>1$ at .1 GHz

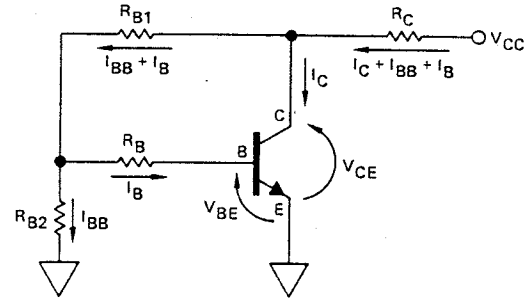
s-parameters, of same transistor with good 4 GHz emitter bypass capacitor. S'_{11} at 4 GHz remains unchanged while $|S_{11}|$ at .1 GHz is greater than 1 indicating conditional stability.

Figure 1.

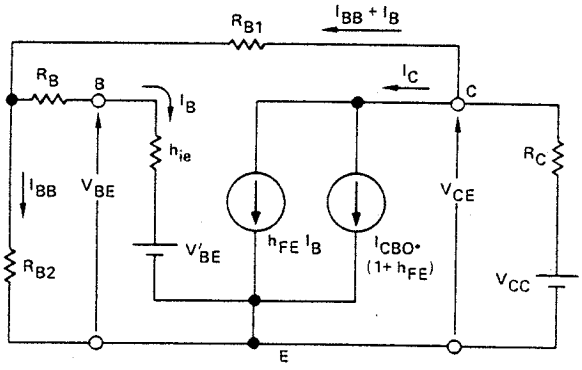
ANALYSIS

In order to best select an optimum bias network, a method of comparison has to be developed. Analysis of transistor bias network instability involves writing a collector current equation in terms of the transistor equivalent circuit and the external bias circuitry. Partial derivatives of the collector current, with respect to the temperature dependent variables, are calculated individually and the resultant stability factors can then be considered simultaneously to predict collector current temperature behavior.

A look at the typical bias circuit of Figure 2a and its dc equivalent circuit in Figure 2b identifies the internal parameters that affect collector current. Since the external resistors have negligible temperature change compared to the transistor, the temperature sensitive parameters are found to be V'_{BE}, I_{CBO}, and h_{FE}.



A. Bias circuit showing only the DC components.



B. The equivalent circuit of Figure 2a is used in DC stability analysis.

NOTES: V'_{BE} is internal to the transistor and has a $-2mV/°C$ temperature coefficient.

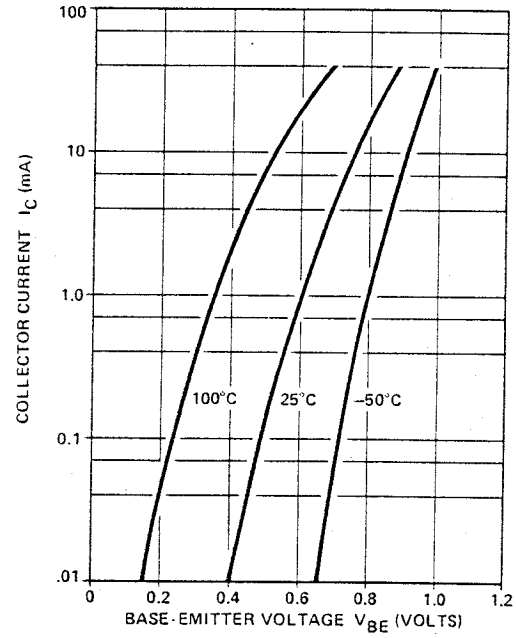
h_{ie} is the hybrid-π input impedance and for Hewlett-Packard microwave transistors is approximately 500 ohms. The exact value is unimportant since h_{ie} is always in series with the larger base bias resistor R_B. It is only included for completeness.

Figure 2.

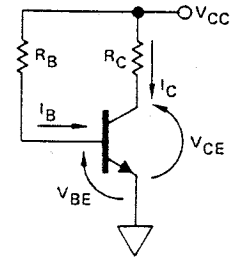
TEMPERATURE SENSITIVE DC PARAMETERS

■ Base Emitter Voltage (V_{BE})

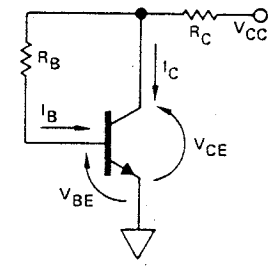
V'_{BE} is the base-emitter voltage. V_{BE} is internal to the transistor and has a negative temperature coefficient of -2 mV/°C. Figure 3a shows a typical silicon PN junction current-voltage relation. Notice the negative shift in threshold voltage for increased temperatures. A bias circuit that fixes a constant voltage on the base, independent of temperature, will find the collector current increasing for increasing temperature. Fortunately, negative voltage feedback will help compensate for V'_{BE} changes as illustrated in Figure 3b and 3c.



A. Typical base-emitter voltage (V_{BE}) vs. collector current (I_C) curve showing the threshold shift due to sensitivity of V'_{BE} = -2 mV/°C.



B. Bias Network that uses no feedback and is sensitive to changes in V'_{BE}, I_{CBO}, and h_{FE}.



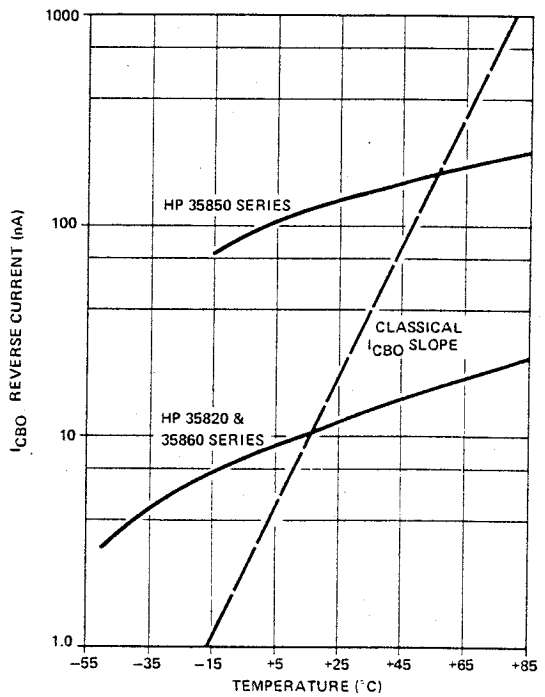
C. Bias network that uses voltage feedback and is less sensitive to changes in V'_{BE}, I_{CBO}, and h_{FE}.

Figure 3.

■ Reverse Collector Current (I_{CBO})

I_{CBO} is the current flowing through a reverse biased PN junction. Classically, this leakage current is expected to double for every 10°C temperature rise in a silicon semiconductor junction.

Microwave transistors have a more complicated reverse current flow. A small component of this current flow is a conventional I_{CBO} term but the major contributor is a surface current that flows across the top of the silicon crystal lattice and this surface current is a more linear function of temperature than the I_{CBO} current. The total reverse current, made up of I_{CBO} and surface components, increases at a rate much less than that which would be expected from an I_{CBO} current alone of the same magnitude. A typical reverse current versus temperature relationship is shown for several HP microwave transistors in Figure 4. The data applies to a collector-base voltage of 10 volts.



Typical reverse current vs. temperature for Hewlett-Packard microwave transistors. For a microwave transistor $I_{CBO} = I_s$ (surface current) + I_j (junction current).

Figure 4.

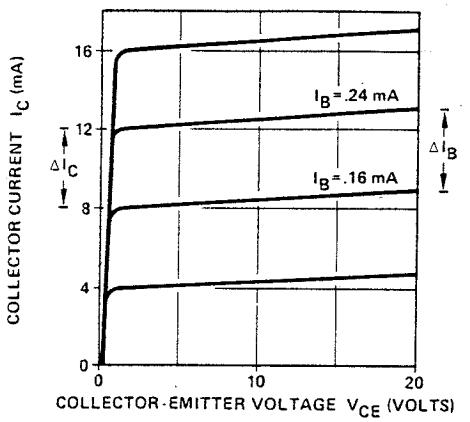
In general, the slope of the I_{CBO} curve for HP microwave transistors remains unchanged with reverse bias. For stability calculations a family of curves, at specified collector to base voltages, can be considered to follow the slope of the curve with intercepts at 25°C corresponding to the data sheet or measured value of I_{CBO}.

■ DC Current Gain (h_{FE})

The typical characteristic curve of Figure 5 shows the collector current versus collector to emitter voltage for a constant base current.

The h_{fe} is defined as the ratio of the change of collector current to the change in base current

$$h_{fe} = \beta = \frac{\Delta I_C}{\Delta I_B}\Bigg|_{V_{CE} = \text{constant}}$$



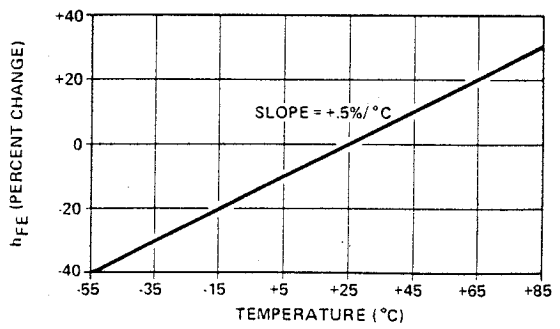
A typical common emitter characteristic curve showing the relationships between base current and collector current.

Figure 5.

h_{FE}, the dc value of the current gain, is defined as the ratio of the collector current (I_C) to base current (I_B).

$$h_{FE} = \beta_{DC} = \frac{I_C}{I_B}\Bigg|_{V_{CE} = \text{constant}}$$

It is this dc value of h_{FE} that is used in the stability calculations and it is found to typically increase linearly with temperature at the rate of 0.5%/°C. Figure 6 shows the temperature dependence of h_{FE}.



Typical percent change in h_{FE} versus temperature (normalized to 25°C).

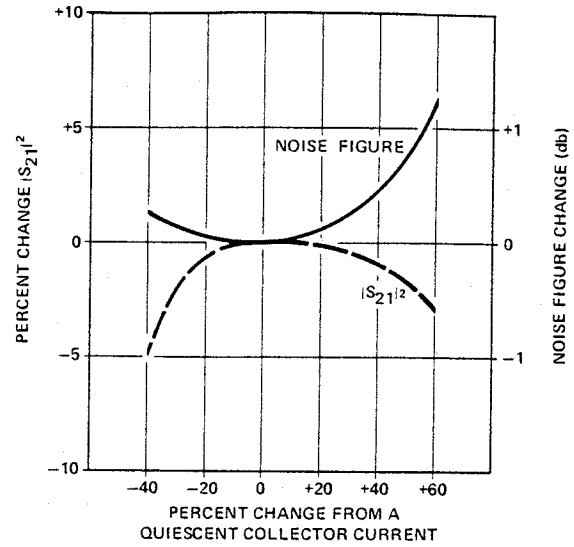
Figure 6.

A look at the four s-parameters and noise figure of HP microwave transistors reveals that $|S_{21}|^2$ and noise figure stand out as the most sensitive parameters to small changes in bias. Also, both of these parameters are stronger functions of collector current (I_C) than of collector to emitter voltage (V_{CE}). This means that if we know something about how $|S_{21}|^2$ and noise figure change with collector current and with temperature, then some constraints can be placed on the bias network to minimize changes in RF performance over a specified temperature range.

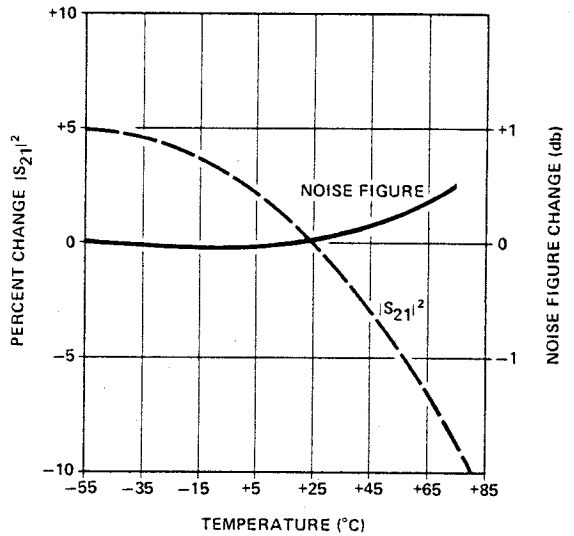
The typical data shown in Figure 7a is normalized to percentage changes in both gain and collector current. The noise figure change is plotted in dB. Although the absolute gain and noise figure are frequency dependent, their sensitivity with respect to collector current (I_C) can be considered frequency independent. Notice that a 20% increase in collector current has a very small effect on either a transistor biased for minimum noise figure or a transistor biased for maximum gain.

Next, a look at some typical changes in noise figure and gain as a function of temperature (Figure 7b) shows that both NF and gain degrade with increasing temperature. We see, for example, that a bias network that can hold the quiescent point such that the current does not increase more than 20% to 60°C will have a 5% degradation in gain or a 0.3 dB increase in noise figure at 60°C due to transistor changes alone. Some temperature compensation could be designed into the bias circuitry by using lower values of collector current at 25°C and allowing the temperature sensitivity of the bias network to offset the temperature sensitivity of the transistor.

It should be pointed out that each amplifier *function* has a different bias requirement. In other words, transistors used in gain stages in which the noise figure or the saturated output power are not critical have a much more relaxed bias stability requirement than, say, a low noise front-end transistor. This can be seen in Figure 7a since $|S_{21}|^2$ has a broad maximum compared to noise figure. A transistor biased for high linear output power must hold its quiescent point such that the 1 dB compression point is not degraded with temperature and so that the maximum power dissipation in the device is not exceeded with increasing temperature.



A. Typical change in performance as a function of collector current variation for a transistor biased at minimum noise figure and a transistor biased at maximum gain.



B. Typical change in performance as a function of temperature variation for a transistor biased at minimum noise figure and a transistor biased at maximum gain (normalized to 25°C).

Figure 7.

SUGGESTED BIAS CIRCUITS

Three bias circuit topologies are shown in Table 1 along with a general expression for the collector current and the calculated dc bias stability factors for V'_{EB}, I_{CBO} and h_{FE}. Most microwave circuit designs, for reasons of noise figure, gain, and RF stability will require a dc grounded emitter; therefore, emitter resistor stabilized circuits will not be considered. The grounded emitter non-stabilized bias circuit (Table 1a) finds very little usage in microwave circuit design since it exhibits the least dc bias stability.

Both circuits in Tables 1b and 1c find widespread usage as bias networks. The voltage feedback circuit uses fewer components and is almost as temperature stable as Table 1c. The addition of R_{B1} and R_{B2} to the voltage feedback circuit does two things. First, it makes all the element values lower in resistance and this makes it more compatible with thin/thick film resistor values. In the voltage feedback circuit the value of R_B would typically be in the range of 30 kΩ to 100 kΩ and these values are difficult to achieve in hybrid integrated circuits. Second, the circuit of 1c can be considered to have a constant base current source, through R_B, and this then allows for trimming, on a production basis, to initially set the collector current to the desired value. The collector current cannot be measured directly since the current in R_c is made up of base current, base bias network current, and collector current. However, since I_c is proportional to V_{CE}, monitoring V_{CE} while adjusting R_B accommodates any value of h_{FE} that will be encountered in HP transistors.

Differences in collector current stability for each topology are compared in Figure 8. It is important to point out that, for the sake of comparison, each circuit was used to bias the transistor to a common quiescent point. This data is typical for frequently encountered microwave bias circuits and is valuable in relative comparisons. Notice that for each of the circuits, the collector current is a positive linear function of temperature. And from Figure 7a, we see that noise figure degradation and gain are negative functions of both collector current and junction temperature.

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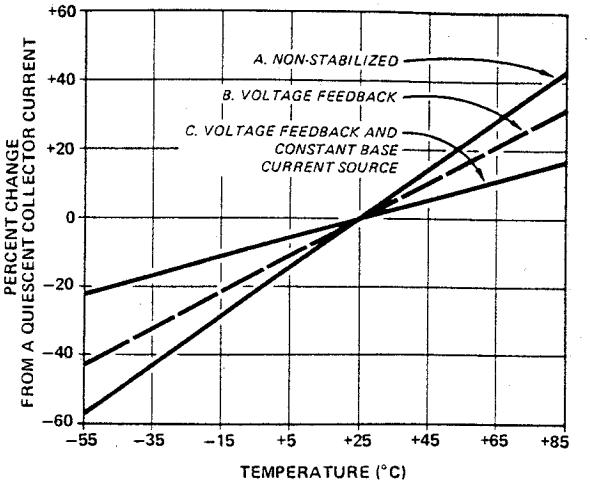
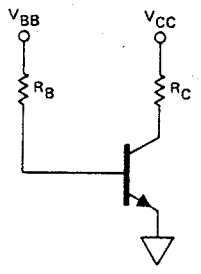
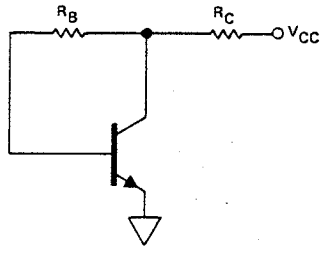


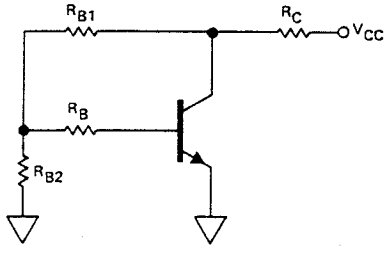
Typical DC stability performance of each bias network (Table 1) used to bias Hewlett-Packard microwave transistors. Graph shows the percent change from a nominal quiescent collector current as a function of temperature (normalized to 25°C).



NON-STABILIZED



VOLTAGE FEEDBACK



VOLTAGE FEEDBACK AND CONSTANT BASE CURRENT SOURCE

Figure 8.

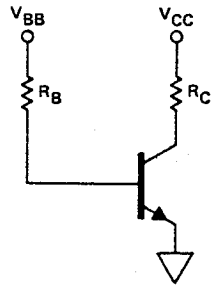
Table 1. Microwave Transistor Stability Factors

Bias networks for DC grounded emitter operation. For each circuit the general expression for the collector current along with the stability factors are given.

The "voltage feedback" circuit of 1B and the "voltage feedback and constant base current" circuit of 1C will provide for temperature stable DC operation and complement the RF Performance of the following Hewlett-Packard transistor series:

HP 35820, HP 35850, HP 35860.

The non-stabilized circuit of 1A is not recommended and is only shown for comparison.



A. NON-STABILIZED

COLLECTOR CURRENT AT ANY TEMPERATURE (I_C)	$\frac{h_{FE}(V_{BB} - V'_{BE})}{(h_{ie} + R_B)} + I_{CBO}(1 + h_{FE})$
I_{CBO} STABILITY FACTOR $\partial I_{CBO} = \frac{\partial I_C}{\partial I_{CBO}}\Big\|_{h_{FE},\, V'_{BE} = \text{constant}}$	$1 + h_{FE}$
V'_{BE} STABILITY FACTOR $\partial V'_{BE} = \frac{\partial I_C}{\partial V'_{BE}}\Big\|_{h_{FE},\, I_{CBO} = \text{constant}}$	$\frac{-h_{FE}}{h_{ie} + R_B}$
h_{FE} STABILITY FACTOR $\partial h_{FE} = \frac{\partial I_C}{\partial h_{FE}}\Big\|_{h_{FE},\, V'_{BE} = \text{constant}}$	$\frac{V_{BB} - V'_{BE}}{h_{ie} + R_B} + I_{CBO}$

USE OF STABILITY FACTORS

$$S_{I_{CBO}} = \frac{\partial I_C}{\partial I_{CBO}}\Big|_{h_{FE},\, V'_{BE} = \text{Constant}}$$

$$S_{V'_{BE}} = \frac{\partial I_C}{\partial V'_{BE}}\Big|_{I_{CBO},\, h_{FE} = \text{Constant}}$$

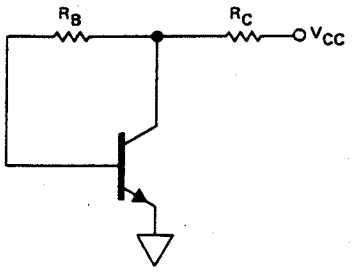
$$S_{h_{FE}} = \frac{\partial I_C}{\partial h_{FE}}\Big|_{I_{CBO},\, V'_{BE} = \text{Constant}}$$

$$\Delta I_C = \frac{\partial I_C}{\partial I_{CBO}} \cdot \Delta I_{CBO} + \frac{\partial I_C}{\partial V'_{BE}} \cdot \Delta V'_{BE} + \frac{\partial I_C}{\partial h_{FE}} \cdot \Delta h_{FE}$$

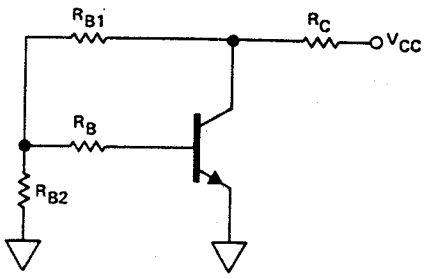
$$\Delta I_C = S_{I_{CBO}} \cdot \Delta I_{CBO} + S V'_{BE} \cdot \Delta V'_{BE} + S_{h_{FE}} \cdot \Delta h_{FE}$$

First calculate the stability factors for V'_{BE}, I_{CBO}, and h_{FE}. Then, to find the change in collector current at any temperature, multiply the change from 25°C of each temperature dependent variable with its corresponding stability factor and sum.

It would appear to be an easy task to further analyze the individual stability factors for minimums in terms of the external circuit resistor values. This is not too easily done since all the factors are inter-related. The stability factors must be considered simultaneously since an optimum set of resistor values to minimize one parameter could grossly increase another.



B. VOLTAGE FEEDBACK



C. VOLTAGE FEEDBACK AND CONSTANT BASE CURRENT SOURCE

$\frac{h_{FE}(V_{CC} - V'_{BE}) + I_{CBO}(1+h_{FE})(h_{ie} + R_B + R_C)}{h_{ie} + R_B + R_C(1+h_{FE})}$	$h_{FE}\left\{\frac{-V'_{BE}A - R_{B2}[(R_C I_{CBO}(1+h_{FE}) - V_{CC})]}{(R_B + h_{ie})A + R_{B2}(h_{FE}R_C + R_C + R_{B1})}\right\} + I_{CBO}(1+h_{FE})$
$\frac{(1+h_{FE})(h_{ie} + R_B + R_C)}{h_{ie} + R_B + R_C(1+h_{FE})}$	$(1+h_{FE}) - \left(\frac{R_{B2} H_{FE} R_C (1+h_{FE})}{A(R_B + h_{ie}) + R_{B2}(h_{FE}R_C + R_C + R_{B1})}\right)$
$\frac{-h_{FE}}{h_{ie} + R_B + R_C(1+h_{FE})}$	$\frac{-h_{FE}A}{(R_B + h_{ie})A + R_{B2}(h_{FE}R_C + R_C + R_{B1})}$
$\frac{(h_{FE}R_C + R_B + h_{ie} + R_C)(V_{CC} - V'_{BE} + KI_{CBO})}{D^2}$ $-R_C\left[\frac{(h_{FE}(V_{CC} - V'_{BE} + KI_{CBO}) + KI_{CBO}}{D^2}\right]$ where: $K = h_{ie} + R_B + R_C$ and $D = h_{FE}R_C + R_B + h_{ie} + R_C$	$h_{FE}\left\{\frac{R_{B2}R_C[(R_{B2}V_{CC} - B) - R_{B2}R_C I_{CBO}(1+h_{FE})]}{D^2}\right\} +$ $\left\{\frac{B - R_{B2}[R_C I_{CBO}(1+h_{FE}) + V_{CC} + h_{FE}R_C I_{CBO}]}{D}\right\} + I_{CBO}$ where: $A = R_{B1} + R_{B2} + R_C$ $B = -V'_{BE}(R_{B1} + R_{B2} + R_C)$ $C = (R_B + h_{ie})(R_{B1} + R_{B2} + R_C)$ $D = C + R_{B2}(h_{FE}R_C + R_C + R_{B1})$

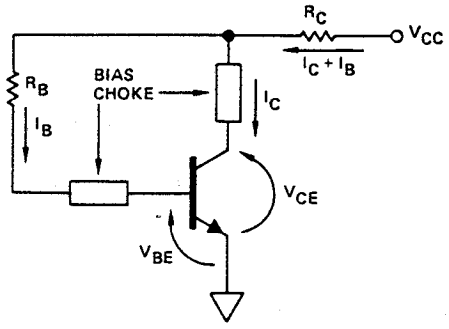
Portions of this Application Note appeared in MicroWaves magazine.

DESIGN EXAMPLES

Some examples of how to go about calculating the resistor values for the two most commonly used grounded emitter bias circuits are given below. The resistor values are calculated and the nearest standard 1% tolerance resistor values are shown. Depending upon the exact application, other tolerance resistors can be used with little or no difference. Also, listed in tabular form, are other resistor values that have been calculated for the indicated quiescent points at a 20 volt supply voltage. Other supply voltages can be calculated accordingly.

For bias circuit designs with HP microwave transistors, assume $h_{fe} = 50$ and neglect h_{ie}.

EXAMPLE 1



1. Determine supply voltage available (V_{CC} = 20V) and transistor operating bias point (10V, 10mA), assume $I_{CBO} = 0$, V_{BE} = .7 volts.

2. Knowing the measured value of h_{FE}, (or assume 50), calculate base current I_B (mA) = I_C (mA)/h_{FE} = 10/50 = .2 mA.

3. Calculate R_B knowing V_{BE} = .7V and V_{CE} = 10V

$$R_B\ (K\Omega) = \frac{V_C - V_{BE}}{I_B} = \frac{(Volts)}{(mA)} = \frac{10 - .7}{.2} = 46.5K\Omega$$

(use R_B = 46.4 KΩ)

4. Calculate R_C

$$R_C\ (K\Omega) = \frac{V_{CC} - V_C}{I_C + I_B} = \frac{(Volts)}{(mA)} = \frac{20 - 10}{10 + .2} = .98K\Omega$$

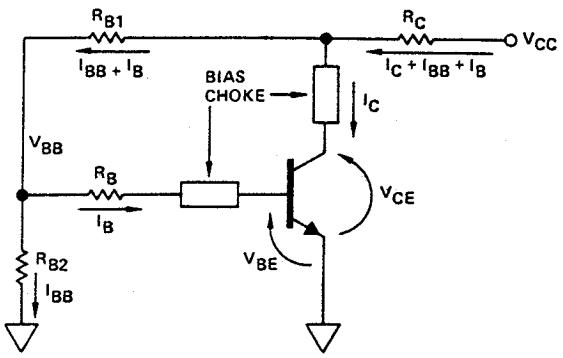
(use R_C = 1 KΩ)

Note that a ± 20% error in assuming a value of h_{FE} will only change I_C ± 1 mA.

5. The general equation for collector current can now be used to check the design using actual calculated resistor values.

6. After the transistor circuit is constructed a quick measurement of V_{CE} will ensure that the device is biased correctly. Since V_{CE} is proportional to $\frac{1}{h_{FE}}$, the base resistor (R_B) can be adjusted accordingly to compensate for manufacturing variations in h_{FE}. This is easily done by varying R_B while monitoring V_{CE} to properly obtain the desired collector current.

EXAMPLE 2



1. Determine supply voltage available (V_{CC} = 20V) and transistor bias operating point (10V, 10mA). Assume $I_{CBO} = 0$, V_{BE} = .7V.

2. Select V_{BB} to be 2V to ensure constant base current source.

3. Knowing the measured value of h_{FE}, (or assume 50), calculate base current I_B (mA) = I_C (mA)/h_{FE} = 10/50 = .2 mA.

4. Calculate R_B knowing V_{BE} = .7V and V_{BB} = 2V

$$R_B\ (K\Omega) = \frac{V_{BB} - V_{BE}}{I_B} = \frac{(Volts)}{(mA)} = \frac{2 - .7}{.2} = 6.5K\Omega$$

(use R_B = 6.81K)

5. Calculate R_{B2} assuming I_{BB} = 1 mA

$$R_{B2}\ (K\Omega) = \frac{V_{BB}}{I_{BB}} = \frac{(Volts)}{(mA)} = \frac{2}{1} = 2K\Omega$$

(use R_{B2} = 1.96K)

6. Now calculate R_{B1} knowing I_B, I_{BB}, V_{BB} and V_{CC}

$$R_{B1}\ (K\Omega) = \frac{V_{CE} - V_{BB}}{I_{BB} + I_B} = \frac{(Volts)}{(mA)} = \frac{10 - 2}{1.2} = 6.66K\Omega$$

(use R_{B1} = 6.19K)

7. Calculate R_C knowing I_C, $I_{BB} + I_B$, V_{CC} and V_{CE}

$$R_C\ (K\Omega) = \frac{V_{CC} - V_{CE}}{I_C + I_{BB} + I_B} = \frac{(Volts)}{(mA)} = \frac{20 - 10}{10 + 1.2} = .893K\Omega$$

(use R_C = 909Ω)

8. The general equation for collector current can now be used to check the design using actual calculated resistor values.

9. After the circuit is designed, R_B may be adjusted to obtain an exact value of I_C.

TABLE OF TYPICAL RESISTOR VALUES FOR INDICATED BIAS (V_{CC} = 20V)

BIAS	h_{FE}	R_B	R_C
10V, 5mA	50	90.9KΩ	1.96KΩ
10V, 10mA	50	46.4KΩ	1KΩ
15V, 15mA	50	46.4KΩ	348Ω

TABLE OF TYPICAL RESISTOR VALUES FOR INDICATED BIAS (V_{CC} = 20V)

BIAS	h_{FE}	R_C	R_B	R_{B1}	R_{B2}
10V, 5mA	50	1.62KΩ	12.1KΩ	7.5KΩ	1.96KΩ
10V, 10mA	50	909Ω	6.81KΩ	6.19KΩ	1.96KΩ
15V, 15mA	50	316Ω	4.22KΩ	10KΩ	1.96KΩ

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