HMMC-5040

As a 20 - 40 GHz Multiplier

Application Note # 50 - Rev A.1

MWTC MARKETING
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1.0 Introduction

This application note describes the use of the HMMC-5040 configured as a harmonic frequency multiplier. Properly configured the HMMC-5040 will amplify harmonic responses which fall in the 20 - 40 GHz passband of the circuit.

This application note provides information necessary to configure the circuit for operation as an even harmonic multiplier or as an odd harmonic multiplier. Typical measured performance data is provided for both types of operation (even and odd) at selected frequencies and operating points as well as temperature stability information.

2.0 Harmonic Multiplier Operation

The HMMC-5040 is a four stage broad band microwave gain block covering the 20 - 40 GHz region. The typical frequency response curve for this circuit is shown in Figure 1. Note the flat gain response and the steep roll off at the band edges. An important design feature for harmonic multiplier operation is that even though the gain rolls off dramatically below 20 GHz, the input return loss remains excellent (better than 10 dB) for input signal frequencies down to DC. This means frequencies below the band pass remain in a 50 ohm system. Any below band signal will be suppressed, but the harmonics which are in band (20 - 40 GHz) will be amplified at the output. This feature makes the HMMC-5040 a good choice for many frequency multiplier applications in the 20 - 40 GHz band.

The HMMC-5040 becomes an effective multiplier through proper biasing of the first stage. The design provides for independent biasing of the first two stages of the circuit. For many applications it is sufficient to separately bias only the first stage, but for some applications additional performance is obtainable by optimizing bias conditions of the second stage as well.

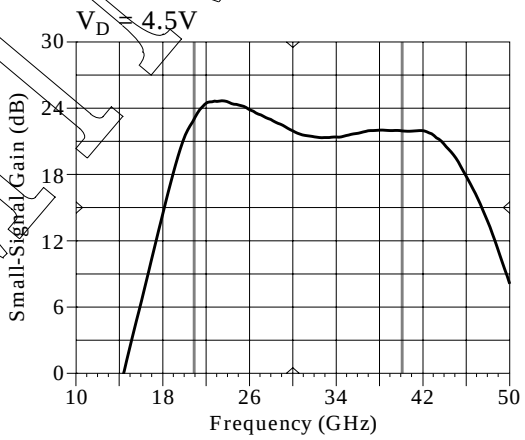

Figure 1.
HMMC-5040 Gain

Many bias schemes may be used to generate and amplify the desired harmonic response of the HMMC-5040. Establishing the bias conditions for multiplier operation depends on the application details such as fundamental frequency, desired multiple frequency, input drive conditions, output signal level, suppression requirements, etc.

The next two sections of this application note provide biasing information and typical measured performance data for the even harmonic and the odd harmonic multiplier configurations.

The RF test circuit used for measurements in this application note is shown in Figure 2.

A 50Ω thru was used to measure path losses and to make sure that the harmonic contribution from the source was negligible.

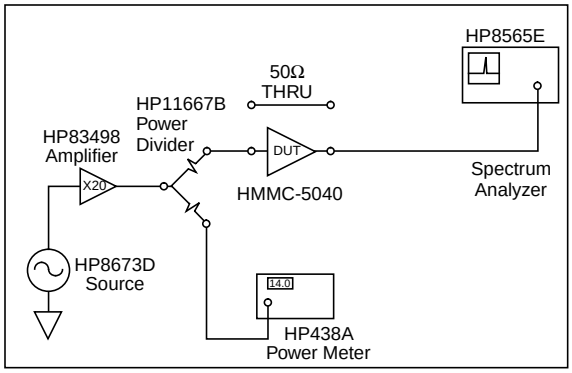

Figure 2.
HMMC-5040 Test Circuit

3.0 Even Harmonics

Doubler - When frequencies between 20 GHz and 26 GHz are desired, the HMMC-5040 used as a doubler will provide conversion gain up to 7 dB and second harmonic output power levels greater than 20 dBm.

At doubled frequencies above 26 GHz the fundamental frequency approaches the lower band edge resulting in increasing fundamental output power and a corresponding decrease in the harmonic power level. This effect is illustrated in Figure 3.

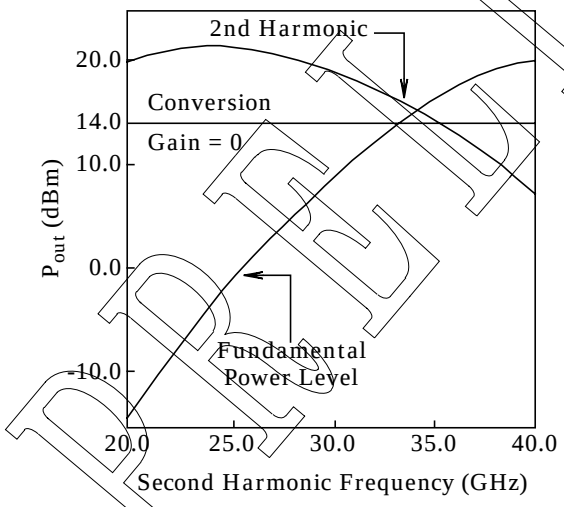

Figure 3.
Doubler Operation

Figure 3 graphically shows the relationship of the second harmonic power level to the fundamental power level of a HMMC-5040 biased as a doubler in the 20 - 40 GHz range. For this plot, 14 dBm is the input power level. Fourteen dBm has been experimentally determined to provide optimum conversion gain in most multiplier configurations.

Configured as a doubler the HMMC-5040 provides maximum conversion gain and good fundamental suppression when multiplied output frequencies between 20 GHz and 26 GHz are desired.

Quad and Beyond - Low frequency oscillators can be used to drive the HMMC-5040 to provide higher order harmonic products which fall in the 20 - 40 GHz range. The 4th, 6th, 8th harmonics and beyond which fall in the pass band of the multiplier, still retain good signal to noise ratios. Figure 4 is a plot of typical even harmonics and their output power levels as a function of input drive levels for a fundamental frequency of 5.5 GHz.

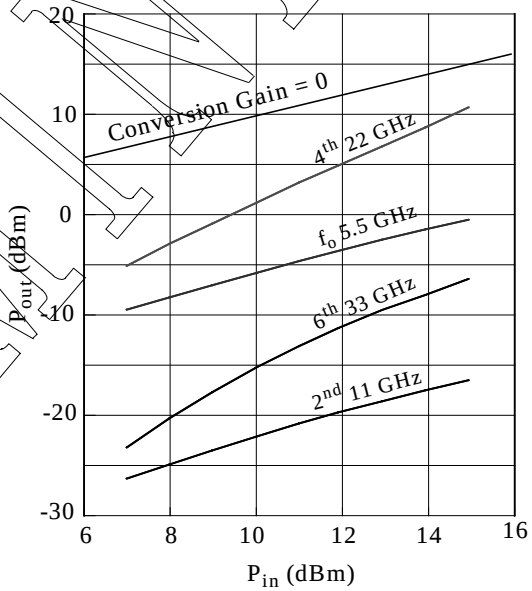

Figure 4.
Even Harmonic Operation

Even Harmonic Biasing - Even harmonics are present when a waveform is not symmetrical. Even harmonics can be increased by biasing the first stage's operating point into a region where the input signal's waveform symmetry is altered. Two possibilities exist for this condition. The first stage can be biased toward forward conduction or biased toward pinchoff. In both cases half of the wave form is distorted, increasing even harmonic content.

Biasing toward forward conduction is less efficient than biasing toward pinchoff because drain

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current is higher, which results in increased power dissipation, higher channel temperatures, and the possibility of reliability problems. Biasing toward pinchoff, on the other hand, increases gate to drain voltage and if high RF drive levels are used, the instantaneous drain to gate voltage could exceed the maximum breakdown voltage (-8 volts for the HMMC-5040). For example, with an input drive level of 14 dBm the instantaneous negative peak voltage is ~1.6 volts (using 50Ω as the input impedance). If the drain is biased to 4.5 volts and the gate is pinched off at -2 volts the instantaneous gate to drain voltage = -8.1 volts.

When the channel of the first stage FET is pinched off, only the positive half cycles of the input wave are presented to the second stage. This essentially results in the first stage becoming a halfwave rectifier. Positive half waves are always rich in even harmonics and the odd harmonics are present only to the extent of other distortion mechanisms.

Figure 5 illustrates biasing the first stage's operating point near pinchoff. A typical loadline is drawn for illustration. When the FET is biased near pinchoff, conduction occurs on positive half cycles but not on the negative half of the cycle, and the output wave form contains only the positive half cycles as shown in the figure. This distorted wave is rich in even harmonics. Input signals, with harmonic frequencies falling in the bandpass of the HMMC-5040, are amplified by the second, third and fourth stages.

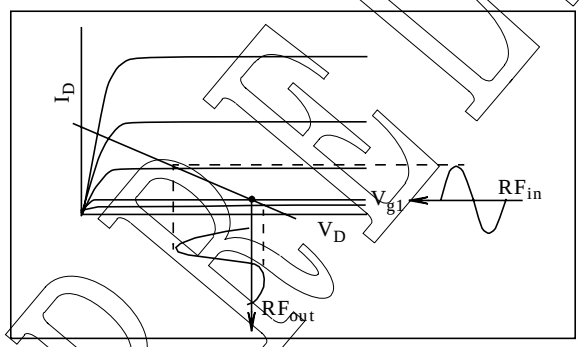

Figure 5.
First Stage Operating Point
Even Harmonic Biasing

Independent biasing of stage one and stage two of the HMMC-5040 can be used as the means to optimize frequency multiplier operation. For most even harmonic multiplier applications it is sufficient to bias the first stage's gate toward pinchoff and normally bias the second, third, and fourth stages as a linear amplifier. The doubler application described in Figures 3 and 4 was biased in this manner. In this application, a single drain voltage at 4.5 volts for all stages was used. Two gate supplies were used: one for stage one, set near pinchoff (V_{g1} ~ = -2.0 volts); and one for stages 2, 3, and 4 which was adjusted until the total drain current = 245 mA, specified as typical for stage 2, 3, and 4 in the data sheet (I_{d1} contribution is low since stage 1 is pinched off).

For each selected frequency and power level V_{g1} was adjusted to provide optimum performance. V_{g1} affects even harmonic performance significantly. Changes to V_{g2} or V_{d1} provided some second order improvement but rarely greater than one dB of output power increase. Odd harmonic suppression could be increased more than 10 dB with minor V_{g2} adjustments but the odd harmonic levels were already fairly low.

4.0 Odd Hamonics

Tripler - HMMC-5040 can be configured to provide good odd harmonic multiples. Conversion gain is lower for odd harmonics than for even harmonics. Certain advantages make odd harmonic operation an attractive solution for some applications. For example, coupling a 13 GHz oscillator to the HMMC-5040 configured as a tripler has been employed, as a cost effective means of generating a 39 GHz signal.

Figure 6 is a plot of the HMMC-5040 tripled output power over the 20 - 40 GHz band. The input power is 14 dBm. The tripled output power remains above 10 dBm to 39 GHz. The fundamental and second harmonic are also plotted to show their relative power level as well, and need to be rescaled on the frequency axis.

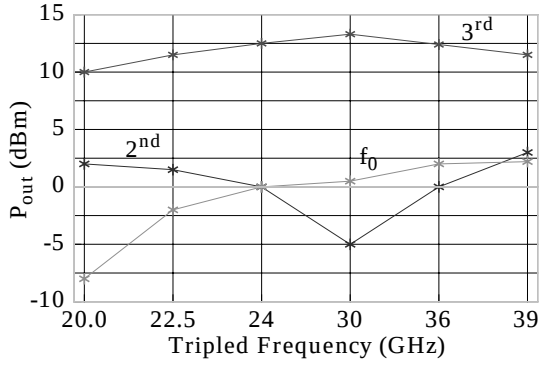

Figure 6.
Tripler Output Power

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Odd Harmonic Biasing - A symmetrical square wave contains only odd harmonics. A balanced square wave can be approximated by clipping a sufficiently large sine wave equally in the positive and negative swings.

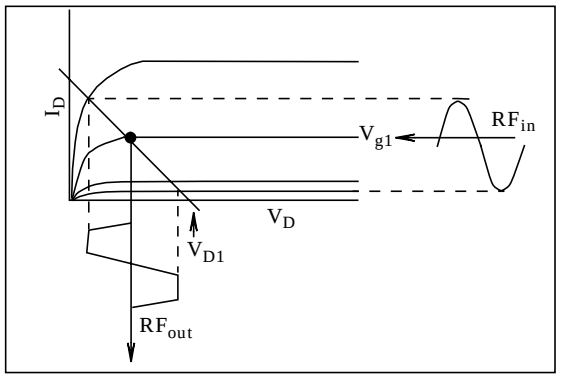

Figure 7.
First Stage Operating Point
Odd Harmonic Biasing

Reducing the drain bias on the first stage (V_{d1}) of the HMMC-5040 and providing a sufficiently high input drive signal will result in the "clipped sine wave" condition (a square wave approximation) presented to the second stage of the circuit (see Figure 7). The positive swinging portion of the input RF wave is clipped as it reaches the forward conducting region of the input FET. The negative swinging portion of the input wave is clipped as the gate field increases and shuts off the FET channel (pinchoff). In this reduced bias condition i.e. lowered V_{d1}, the position of the quiescent operating point is important for two reasons:

1. Selection of the gate bias voltage (V_{g1}) affects the symmetry of the clipped sine wave and thus the undesired even harmonic content. Figure 7 illustrates the importance of V_{g1} is establishing this symmetry.
2. Reducing the bias level (V_{d1}) to insure clipping of the RF input wave results in reduced gain for this stage and a corresponding gain reduction through the circuit, i.e., there is a trade off between lowering V_{d1} to improve odd harmonics through more clipping and between reducing the overall gain of the circuit by lowering V_{d1}.

Complex bias schemes can be devised to optimize odd harmonic content and suppress unwanted multiples, but for many odd harmonic applications a very simple bias approach is sufficient: All the drains are connected together ($V_{d1,2,3,4}$) and all the gates are connected together ($V_{g1,2,3,4}$).

Since the first stage (V_{d1}) is biased down, the full gain potential of stages 2,3,&4 (the remaining circuit) cannot be realized, so RF gain is not sacrificed by lowering V_d for the remaining stages. When V_{g1} is adjusted to obtain waveform symmetry it's value will be a reasonable gate bias for the other three stages as well.

The procedure used to bias the HMMC-5040 as a tripler and provide the measurements for figure 6 is described as follows: The test circuit shown in Figure 2 was used. A single gate supply and a single drain supply was used as described above. First, the gate was set to -1 volt. Next the drain supply was set to 3 volts. For each frequency tested the input power was set to 14 dBm and the spectrum analyzer was adjusted to show the second and third harmonic. The gate voltage was lowered to peak the third harmonic, then the drain voltage was adjusted to an optimum level. Small changes in the gate voltage, at this point, result in second harmonic suppression without significant lowering of the third harmonic. The bias levels were slightly different for each frequency, the drain voltage varied from 2.3 to 3.5 volts and the gate voltage range was -0.6 to -0.8 volts.

5.0 Temperature Stability

Thermal performance was measured in odd and even multiplier configurations. In all cases power output was measured as a function of input power, i.e., input power levels were 7 to 20 dBm in 1 dB steps. Measurements were made at three different ambient temperatures: 4˚C, 25˚C, and 75˚C. In all cases where output power was greater than 0 dBm, amplitude variations were better than 0.06 dB/˚C. The best thermal performance was in doubler configuration where output power levels were above 20 dBm the thermal performance was better than 0.03 dB/˚C.

For additional information please contact your local HP field sales office.

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