HPMX-3003
Demonstration Circuit Board

10/20/95 M. R.

Thank you for your interest in Hewlett-Packard's Cerberus GaAs LNA/Switch/PA MMIC. We hope the enclosed demonstration circuit board will help you meet your circuit design and performance goals.

There are a few simple guidelines to follow to get maximum performance from the board. When using the board **it is strongly recommended that you do not exceed the maximum IC voltage ratings shown on the data sheets**. Drain bias for both the PA and LNA sections of the MMIC should be set to +3 to +5 Volts. The gate bias voltages to the power amplifier section should be adjusted separately to match data sheet specified drain currents.

Figure 1, below, shows the pinout of the DC power and switch control connector.

Figure 2 shows a typical test set up for checking the Switch portion of the MMIC. A scalar network analyzer can be used to measure VSWR, insertion loss (through the "on" switch) and isolation (to the "off" switch). The switch is operated by -3 to -5V control signals applied to C1 and C2.

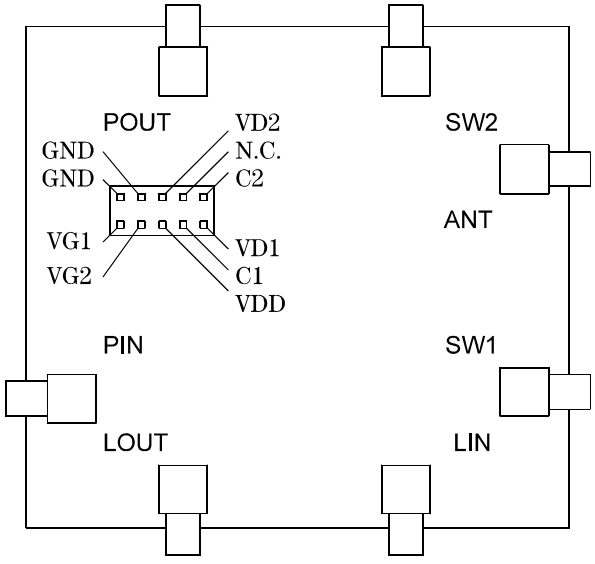

Figure 1. Board layout showing pinout of power supply connector.

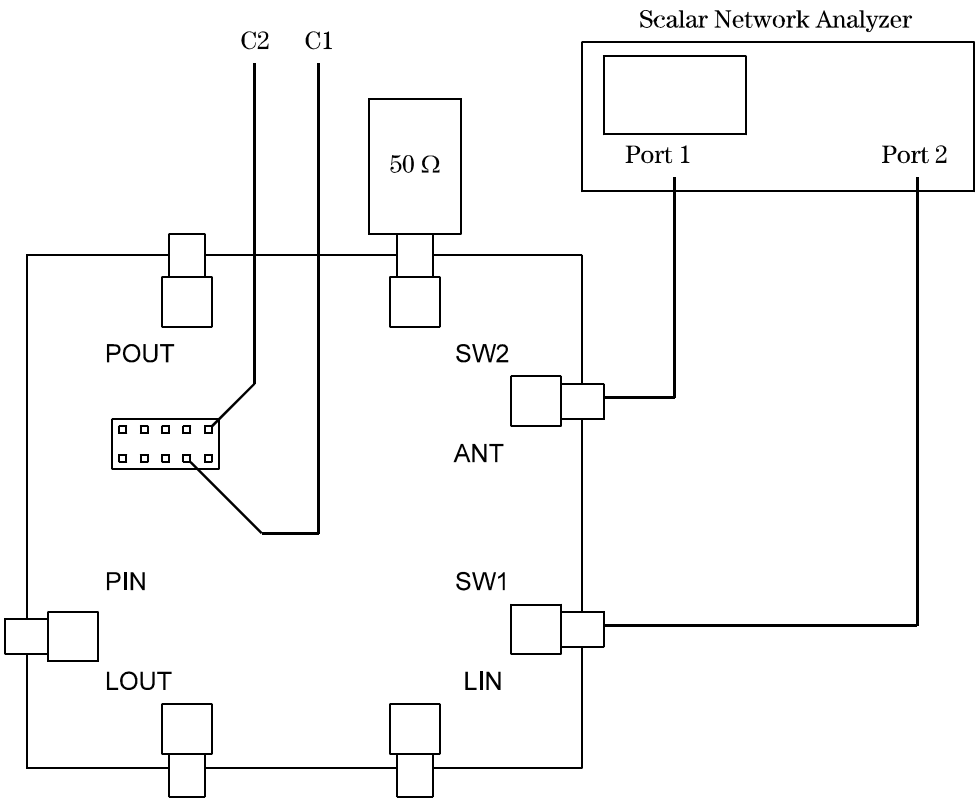

Figure 2: Test set-up for checking the operation of the switch section of the MMIC.

Figures 3, 4, and 5 show test set-ups for the PA. **This is a depletion mode GaAs MMIC so it is important to always apply gate bias before drain bias!** Set the gate bias to about -2 V on pins VG1 and VG2, then apply V_d of +3 to +5 V to pins VD1 and VD2. Slowly raise the gate bias to approximately -0.75 V until I_d is about 400-500 mA.

Figure 3 shows a test equipment set-up for testing the power amplifier stage of the IC. Again, a scalar network analyzer can be used to measure gain, isolation and VSWR.

Figure 4 shows a test set-up for P1dB measurements. Use a dual power meter with a directional coupler to measure the power applied to the input and coming from the output of the amplifier. Start with a low level input signal to ensure operation in the linear mode, then increase power until the gain calculated as the ratio of output to input power is reduced by 1 dB. The output power level at that point is P1dB.

Figure 5 shows a test set-up for measuring power amplifier IP3.

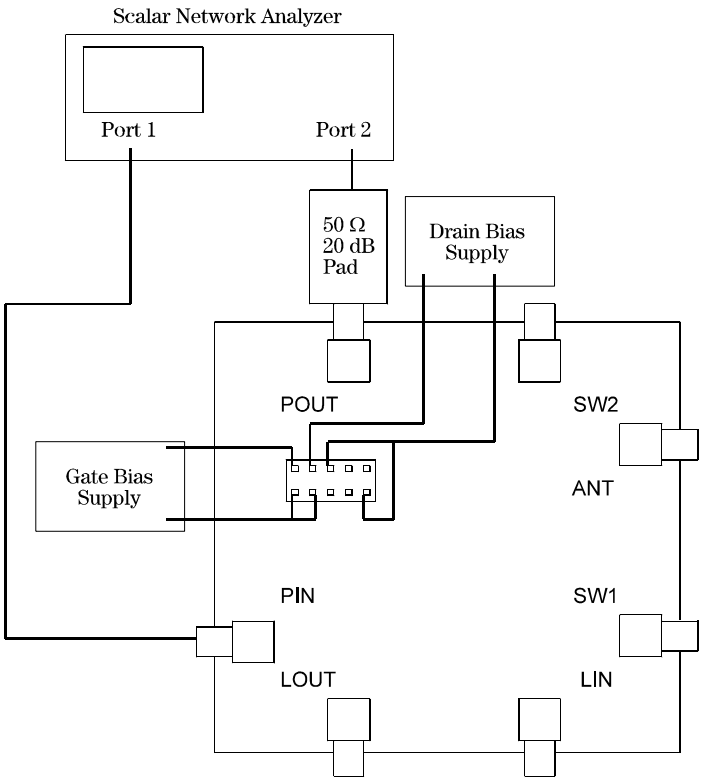

Figure 3: Test set-up for power amplifier gain, VSWR and isolation.

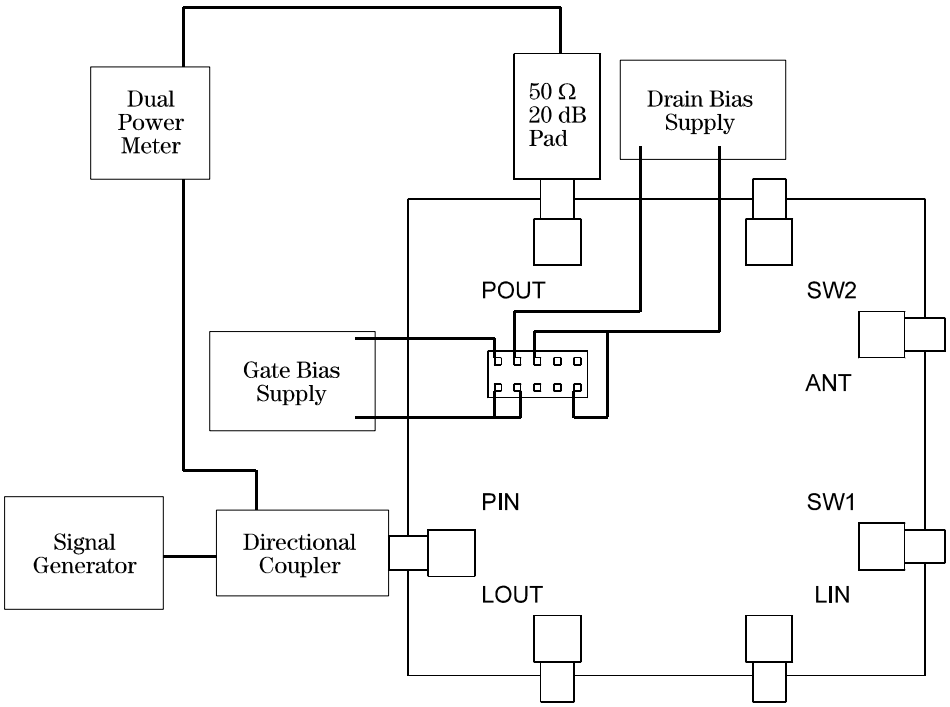

Figure 4: Test set-up for power amplifier stage gain and P1dB

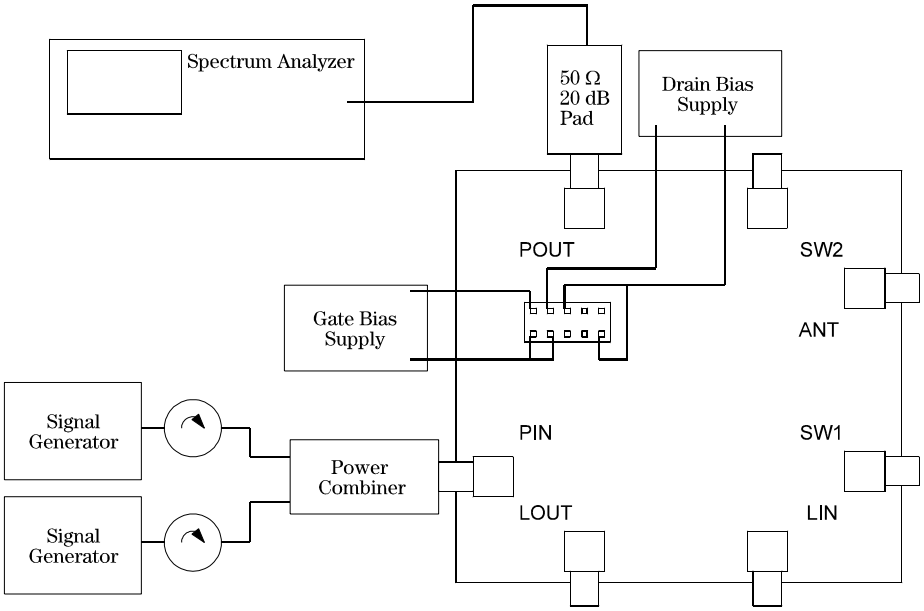

Figure 5: Test set-up for checking power amplifier IP3

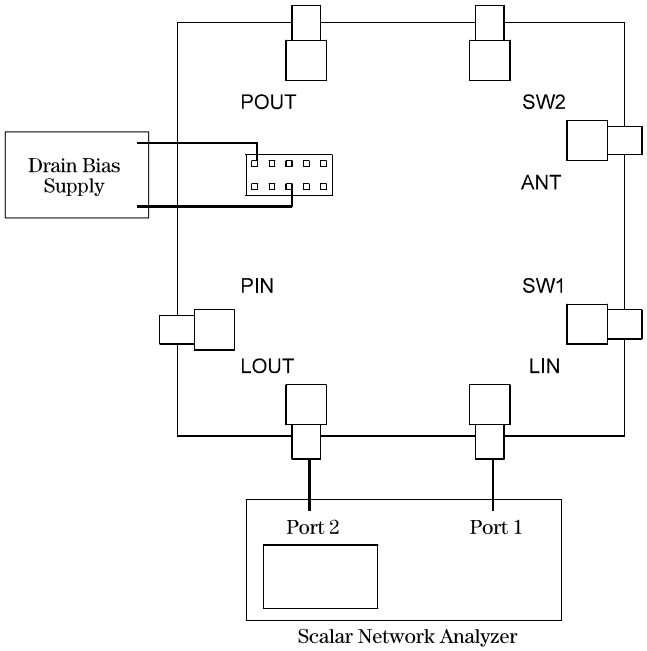

Figure 6: Test set-up for checking LNA VSWR, gain, and isolation

Figure 6, above shows a test-set-up for checking the performance of the LNA section of the MMIC. The set-up allows checking the VSWR, gain and isolation of the LNA. The LNA requires just a single supply voltage of 3 to 5 volts applied to pin VDD.

Finally, a noise figure test set can be used in place of the network analyzer in figure 6 to measure the noise figure of the LNA.