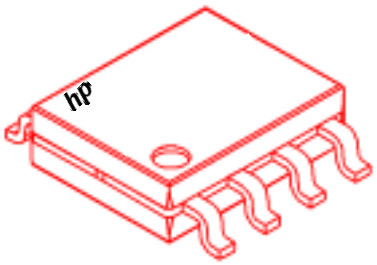
DC - 12 GHz Packaged High Efficiency Divide-by-4 Prescaler

Technical Data

HMMC-3124



Package Type:	8-lead SSOP Plastic
Package Dimensions:	4.9 × 3.9 mm Typ.
Package Thickness:	1.55 mm Typ.
Lead Pitch:	1.25 mm Nom.
Lead Width:	0.42 mm Nom.

Features

- **Wide Frequency Range: 0.2–12 GHz**
- **High Input Power Sensitivity: On-chip pre- and post-amps -15 to +10 dBm (1–8 GHz) -10 to +8 dBm (8–10 GHz) -5 to +2 dBm (10–12 GHz)**
- **P_{out}: 0 dBm (0.5 V_{p-p})**
- **Low Phase Noise: -153 dBc/Hz @ 100 kHz Offset**
- **(+) or (-) Single Supply Bias Operation**
- **Wide Bias Supply Range: 4.5 to 6.5 volt operating range**
- **Differential I/0 with on-chip 50Ω matching**

Description

The HMMC-3124 is a packaged GaAs HBT MMIC prescaler which offers DC to 12 GHz frequency translation for use in communications and EW systems incorporating high-frequency PLL oscillator circuits and signal-path down conversion applications. The prescaler provides a large input power sensitivity window and low phase noise.

Absolute Maximum Ratings[1]

(@ T_A=25°C, unless otherwise indicated)

Symbol	Parameters/Conditions	Min.	Max.	Units
V_{CC}	Bias Supply Voltage		+7	volts
V_{EE}	Bias Supply Voltage	-7		volts
$\lvert V_{CC} - V_{EE} \rvert$	Bias Supply Delta		+7	volts
V_{Logic}	Logic Threshold Voltage	V_{CC}-1.5	V_{CC}-1.2	volts
$P_{in(CW)}$	CW RF Input Power		+10	dBm
V_{RFin}	DC Input Voltage (@ RFin or RF_{in} Ports)		$V_{CC} \pm 0.5$	volts
T_{BS}[2]	Backside Operating Temp.	-40	+85	°C
T_{st}	Storage Temperature	-65	+165	°C
T_{max}	Maximum Assembly Temp. (60 seconds max.)		310	°C

[1] Operation in excess of any parameter limit (except T_{BS}) may cause permanent damage to the device.

[2] MTTF >1×10^6 hours @ T_{BS} <85°C. Operation in excess of maximum operating temperature (T_{BS}) will degrade MTTF.

DC Specifications/Physical Properties

(T_A = 25°C, V_{CC} - V_{EE} = 5.0 volts, unless otherwise listed)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
V_{CC} - V_{EE}	Operating bias supply difference[1]	4.5	5.0	6.5	volts
$\|I_{CC}\|$ or $\|I_{EE}\|$	Bias supply current	34	40	46	mA
$V_{RFin(q)}$ $V_{RFout(q)}$	Quiescent DC voltage appearing at all RF ports		V_{CC}		volts
V_{Logic}	Nominal ECL Logic Level (V_{Logic} contact self-bias voltage, generated on-chip)	V_{CC} - 1.45	V_{CC} -1.32	V_{CC} -1.25	volts

[1] Prescaler will operate over full specified supply voltage range. V_{CC} or V_{EE} not to exceed limits specified in Absolute Maximum Ratings section.

RF Specifications

(T_A = 25°C, Z_0 = 50Ω, V_{CC} - V_{EE} = 5.0 volts)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$f_{in(max)}$	Maximum input frequency of operation	12	14		GHz
$f_{in(min)}$	Minimum input frequency of operation[1] (P_{in} = -10 dBm)		0.2	0.5	GHz
$f_{Self\text{-}Osc.}$	Output Self-Oscillation Frequency[2]		3.4		GHz
P_{in}	@ DC, (Square-wave input)	-15	>-25	+10	dBm
	@ f_{in} = 500 MHz, (Sine-wave input)	-15	>-20	+10	dBm
	f_{in} = 1 to 8 GHz	-15	>-20	+10	dBm
	f_{in} = 8 to 10 GHz	-10	>-15	+5	dBm
	f_{in} = 10 to 12 GHz	-5	>-10	-1	dBm
RL	Small-Signal Input/Output Return Loss (@f_{in}< 10 GHz)		15		dB
S_{12}	Small-Signal Reverse Isolation (@f_{in}<10 GHz)		30		dB
φ_N	SSB Phase noise (@ P_{in} = 0 dBm, 100kHz offset from a f_{out} = 1.2 GHz Carrier)		-153		dBc/Hz
Jitter	Input signal time variation @ zero-crossing (f_{in} = 10 GHz, P_{in} = -10 dBm)		1		ps
T_r or T_f	Output transition time (10% to 90% rise/fall time)		70		ps
P_{out}[3]	@ f_{out} < 1 GHz	-2.0	0.0		dBm
	@ f_{out} = 2.5 GHz	-3.5	-1.5		dBm
	@ f_{out} = 3.0 GHz	-4.5	-2.5		dBm
$\|V_{out(p\text{-}p)}\|$[4]	@ f_{out} <1 GHz		0.5		volts
	@ f_{out} = 2.5 GHz		0.42		volts
	@ f_{out} = 3.0 GHz		0.37		volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} 10 GHz, Unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)		-50		dBm
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 10 GHz, Both RF_{out} & $\overline{RF}_{out}$ **terminated**)		-55		dBm
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 12 GHz, P_{in} = 0 dBm, Referred to $P_{in}(f_{in})$)		-30		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 3.0 GHz, Referred to $P_{out}(f_{out})$)		-25		dBc

[1] For sine-wave input signal. Prescaler will operate down to D.C. for square-wave input signal. Minimum divide frequency limited by input slew-rate.

[2] Prescaler can exhibit this output signal under bias in the absence of an RF input signal. This condition can be eliminated by use of the Input DC offset technique described on page 3.

[3] Fundamental of output square wave's Fourier Series.

[4] Square wave amplitude calculated from P_{out}.

Applications

The HMMC-3124 is designed for use in high frequency communications, microwave instrumentation, and EW radar systems where low phase-noise PLL control circuitry or broad-band frequency translation is required.

Operation

The device is designed to operate when driven with either a single-ended or differential sinusoidal input signal over a 200 MHz to 12 GHz bandwidth. Below 200 MHz the prescaler input is "slew-rate" limited, requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to DC when driven with a square-wave. AC coupling at P_{in} 5 (RF_{in}) is recommended for most applications.

The device can be operated from either a single positive or single negative supply. For positive supply operation V_{CC} pins are nominally biased at any voltage in the +4.5 to +6.5 volt range with P_{in} 8 (V_{EE}) grounded. For negative bias operation V_{CC} pins are typically grounded and a negative voltage between -4.5 to -6.5 volts is applied to P_{in} 8 (V_{EE}).

Input DC Offset

To prevent false triggers or self-oscillation conditions, apply a 20 to 100 mV DC offset voltage between the RF_{in} and $\overline{RF_{in}}$ ports. This prevents noise or spurious low level signals from triggering the divider.

GaAs MMICs are ESD sensitive. Proper precautions should be used when handling these devices.

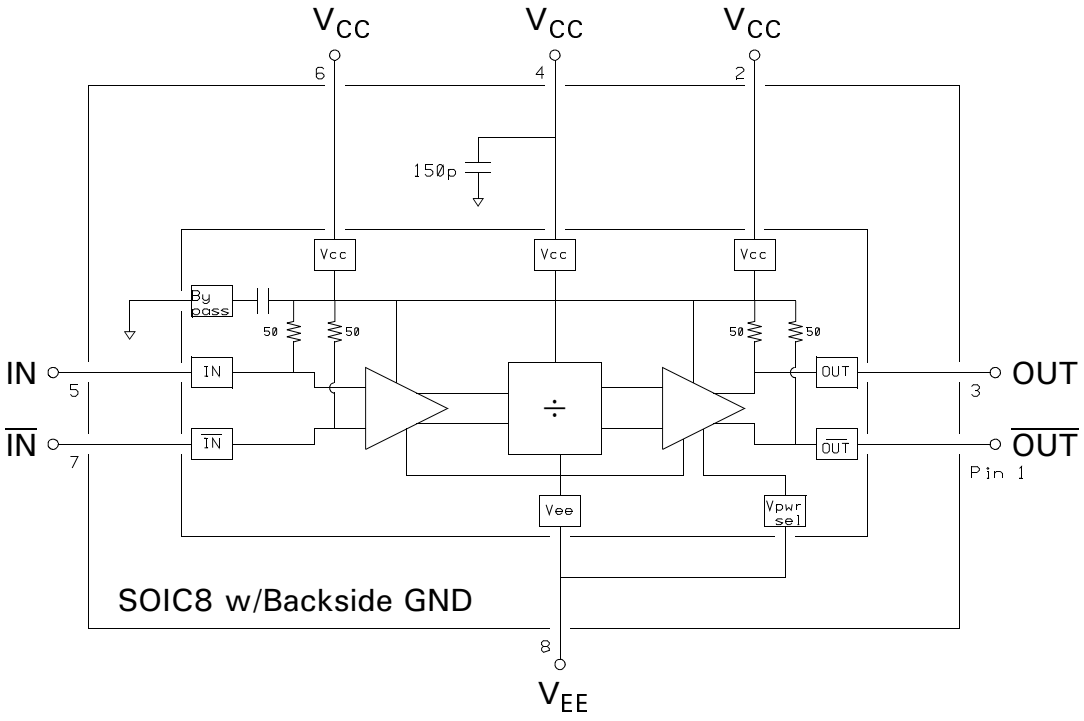
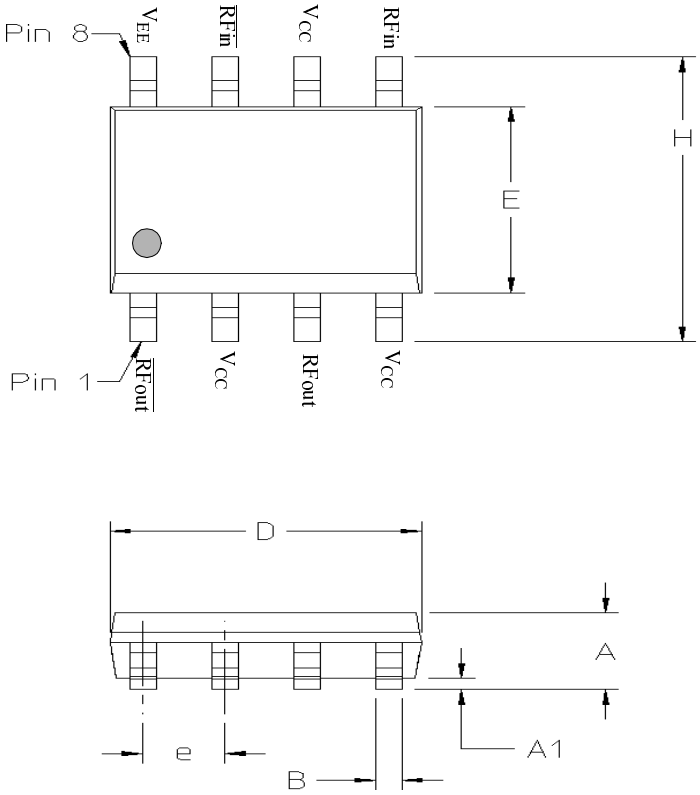


Figure 1.
Simplified Schematic



Notes:

- **All dimensions in millimeters.**
- **Refer to JEDEC Outline MS-012 for additional tolerances**

SYMBOL	MIN.	MAX.
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	.025
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.27
a	0°	8°

- Exposed heat slug area on pkg bottom = 2.67 × 1.65.

Figure 2.
Package & Dimensions

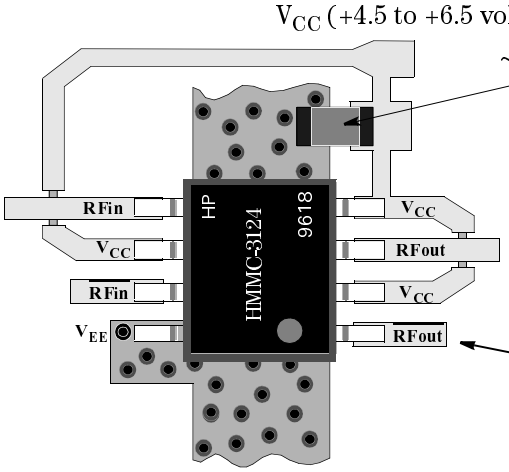


Figure 3.
Assembly Diagram
(Single-Supply, positive-bias configuration shown)

Supplemental Data:

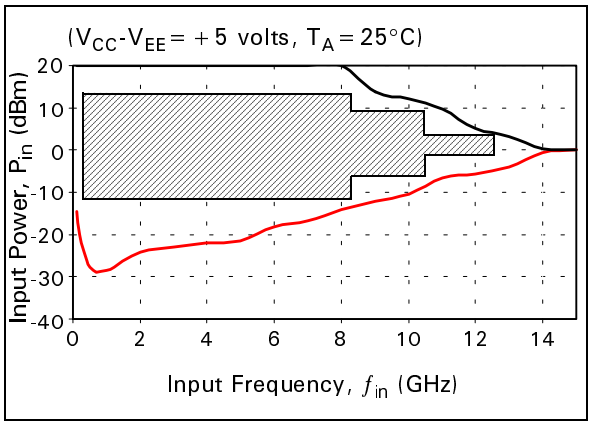


Figure 4.
Typical Input
Sensitivity Window

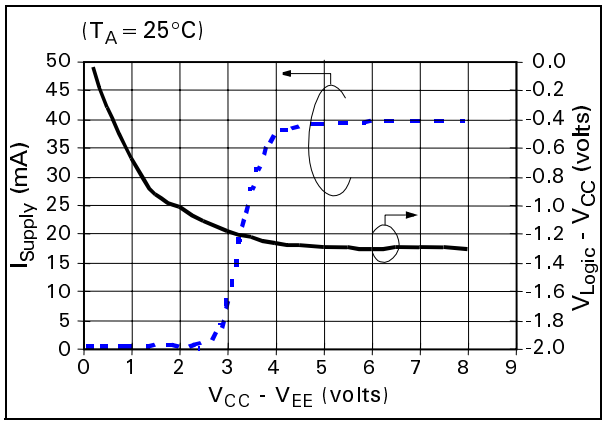


Figure 5.
Typical Supply Current & V_{Logic}
vs. Supply Voltage

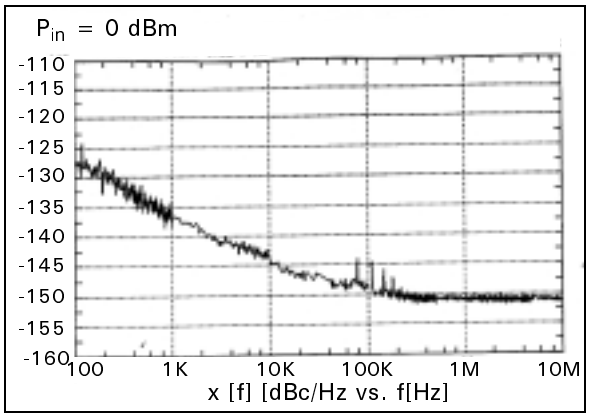


Figure 6.
Typical Phase
Noise Performance

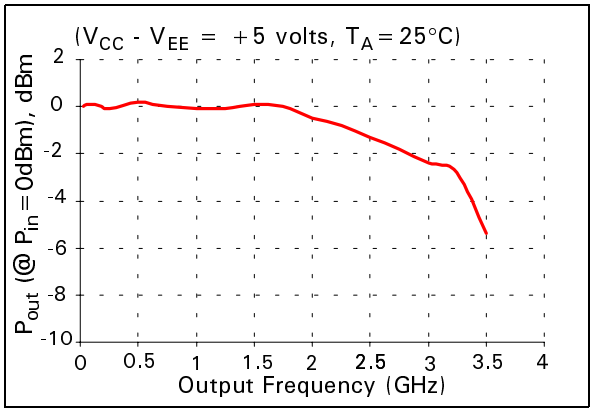


Figure 7.
Typical Output Power vs. Output
Frequency, f_{out} (GHz)

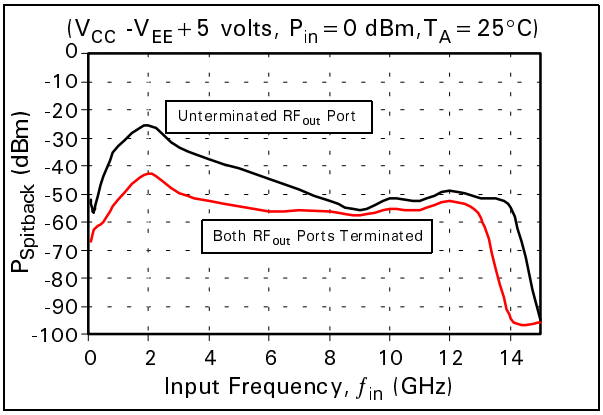


Figure 8.
Typical "*Spitback*" Power
P(f_{out}) appearing at RF input port

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term *typical* refers to the 50th percentile performance. For additional information contact your local HP sales representative.

Notes: