

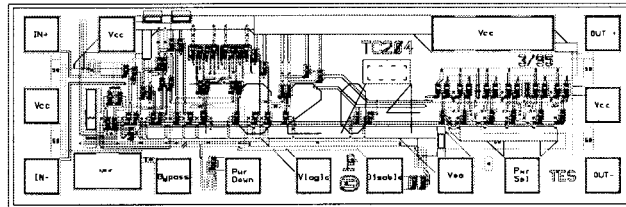
DC – 16 GHz GaAs HBT MMIC Divide-by-2 Prescaler

Technical Data

HMMC-3002

Features

- **Wide Frequency Range:**
0.2 - 16 GHz
- **High Input Power Sensitivity:**
On-chip pre- and post-amps
-20 to +10 dBm (1 - 10 GHz)
-15 to +10 dBm (10 - 12 GHz)
-10 to +5 dBm (12 - 15 GHz)
- **Dual-mode P_{out}: (Chip Form)**
0 dBm [0.5 V_{p-p}] @ 60 mA
+6.0 dBm [0.99 V_{p-p}] @ 80 mA
- **Low Phase Noise:**
-153 dBc/Hz @ 100 kHz Offset
- **(+) or (-) Single Supply Bias Operation**
- **Wide Bias Supply Range:**
4.5 to 6.5 volt operating range
- **Differential I/O with on-chip 50 Ω matching**



Chip Size: 1330 x 440 μm (52.4 x 17.3 mils)
 Chip Size Tolerance: ±10 μm (±0.4 mils)
 Chip Thickness: 127 ± 15 μm (5.0 ± 0.6 mils)
 Pad Dimensions: 70 x 70 μm (2.8 x 2.8 mils)

Description

The HMMC-3002 GaAs HBT MMIC Prescaler offers DC to 16 GHz frequency translation for use in communications and EW systems incorporating high-frequency PLL oscillator circuits and signal-path down conversion applications. The prescaler provides a large input power sensitivity window and low phase noise. In addition to the features listed above the device offers input disable and circuit power-down contact pads to eliminate any self-oscillation condition or reduced power consumption.

Absolute Maximum Ratings^[1]

Symbol	Parameters/Conditions	Units	Min.	Max.
V _{CC}	Bias Supply Voltage	volts		+7
V _{EE}	Bias Supply Voltage	volts	-7	
V _{CC} - V _{EE}	Bias Supply Delta	volts	+7	
V _{Disable}	Pre-amp Disable Voltage	volts	V _{EE}	V _{CC}
V _{PwrDwn}	Prescaler Power-Down Voltage	volts	V _{EE}	V _{CC}
V _{Logic}	Logic Threshold Voltage	volts	V _{CC} -1.5	V _{CC} -1.2
P _{in(CW)}	CW RF Input Power	dBm		+10
V _{RFin}	DC Input Voltage (@ RFin or \overline{RFin} Ports)	volts		V _{CC} ± 0.5
T _{BS} ^[2]	Backside Operating Temp	°C	-40	+85
T _{STG}	Storage Temperature	°C	-65	+165
T _{max}	Maximum Assembly Temp (60 seconds max.)	°C		310

Notes:

1. Operation in excess of any parameter limit (except T_{BS}) may cause permanent damage to the device.
2. MTTF > 1 x 10⁶ hours @ T_{BS} < 85°C. Operation in excess of maximum operating temperature (T_{BS}) will degrade MTTF.

DC Specifications/Physical Properties^[1], ($T_A = 25^\circ\text{C}$, $V_{CC} - V_{EE} = 5.0\text{ V}$ unless otherwise listed)

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
$V_{CC} - V_{EE}$	Operating Bias Supply Difference ^[1]	volts	4.5	5.0	6.5
$ I_{CC} $ or $ I_{EE} $	Bias Supply Current (HIGH Output Power Configuration ^[2] : $V_{PwrSel} = V_{EE}$)	mA	68	80	92
	Bias Supply Current (LOW Output Power Configuration ^[2] : $V_{PwrSel} = \text{open}$)	mA	51	60	69
$V_{RFIn(q)}$ $V_{RFout(q)}$	Quiescent DC Voltage appearing at all RF Ports	volts		V_{CC}	
V_{Logic}	Nominal ECL Logic Level (V_{Logic} contact self-bias voltage, generated on-chip)	volts	$V_{CC} - 1.45$	$V_{CC} - 1.35$	$V_{CC} - 1.25$
$I_{EE(off)}$	Residual Bias Supply Current ($V_{PwrDwn} = V_{CC}$)	mA		6	

Notes:

- Prescaler will operate over full specified supply voltage range. V_{CC} or V_{EE} not to exceed limits specified in Absolute Maximum Ratings section.
- High output power configuration: $P_{out} = +6.0\text{ dBm}$ [$V_{out} = 0.99 V_{p-p}$], Low output power configuration: $P_{out} = 0\text{ dBm}$ [$V_{out} = 0.5 V_{p-p}$].

HMMC-3002 ($\div 2$) RF Specifications, ($T_A = 25^\circ\text{C}$, $Z_O = 50\Omega$, $V_{CC} - V_{EE} = 5.0\text{ V}$)

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
$f_{in(max)}$	Maximum input frequency of operation	GHz	16	18	
$f_{in(min)}$	Minimum input frequency of operation ^[1] ($P_{in} = -10\text{ dBm}$)	GHz		0.2	0.5
$f_{Self-Osc.}$	Output Self-Oscillation Frequency ^[2]	GHz		6.8	
P_{in}	@ DC, (Square-wave input)	dBm	-15	>-25	+10
	@ $f_{in} = 500\text{ MHz}$, (Sine-wave input)	dBm	-15	>-20	+10
	$f_{in} = 1\text{ to }10\text{ GHz}$	dBm	-15	>-25	+10
	$f_{in} = 10\text{ to }12\text{ GHz}$	dBm	-10	>-15	+10
	$f_{in} = 12\text{ to }15\text{ GHz}$	dBm	-4	>-10	+4
RL	Small-Signal Input/Output Return Loss (@ $f_{in} < 12\text{ GHz}$)	dB		15	
S_{12}	Small-Signal Reverse Isolation (@ $f_{in} < 12\text{ GHz}$)	dB		30	
ϕ_N	SSB Phase Noise (@ $P_{in} = 0\text{ dBm}$, 100 kHz offset from a $f_{out} = 1.2\text{ GHz}$ Carrier)	dBc/Hz		-153	
Jitter	Input Signal Time Variation @ Zero-Crossing ($f_{in} = 10\text{ GHz}$, $P_{in} = -10\text{ dBm}$)	ps		1	
T_r or T_f	Output Edge Speed (10% to 90% rise/fall time)	ps		70	

Notes:

- For sine-wave input signal. Prescaler will operate down to D.C. for square-wave input signal. Minimum divide frequency limited by input slew-rate.
- Prescaler may exhibit this output signal under bias in the absence of an RF input signal. This condition may be eliminated by use of the Pre-amp Disable ($V_{Disable}$) or Prescaler Power-Down (V_{PwrDwn}) features, or the Differential Input de-biasing technique.

HMMC-3002 RF Specifications, High Output Power Operating Mode^[1] ($T_A = 25^\circ\text{C}$, $Z_0 = 50\Omega$, $V_{CC} - V_{EE} = 5.0\text{ V}$)

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
P_{out}	@ $f_{\text{out}} < 1\text{ GHz}$	dBm	4.0	6.0	
	@ $f_{\text{out}} = 2.5\text{ GHz}$	dBm	3.5	5.5	
	@ $f_{\text{out}} = 5\text{ GHz}$	dBm	2.0	4.0	
$ V_{\text{out(p-p)}} $	@ $f_{\text{out}} < 1\text{ GHz}$	volts	0.79	0.99	
	@ $f_{\text{out}} = 2.5\text{ GHz}$	volts	0.74	0.94	
	@ $f_{\text{out}} = 5\text{ GHz}$	volts	0.63	0.79	
P_{Spitback}	f_{out} power level appearing at RFin or $\overline{\text{RFin}}$ (@ $f_{\text{in}} = 12\text{ GHz}$, Unused RFout or $\overline{\text{RFout}}$ unterminated)	dBm		-48	
	f_{out} power level appearing at RFin or $\overline{\text{RFin}}$ (@ $f_{\text{in}} = 12\text{ GHz}$, Both RFout & $\overline{\text{RFout}}$ terminated)	dBm		-68	
P_{feedthru}	Power level of f_{in} appearing at RFout or $\overline{\text{RFout}}$ (@ $f_{\text{in}} = 12\text{ GHz}$, $P_{\text{in}} = 0\text{ dBm}$, Referred to $P_{\text{in}}(f_{\text{in}})$)	dBc		-30	
H_2	Second harmonic distortion output level (@ $f_{\text{out}} = 3.0\text{ GHz}$, Referred to $P_{\text{out}}(f_{\text{out}})$)	dBc		-25	

Low Output Power Operating Mode^[2]

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
P_{out}	@ $f_{\text{out}} < 1\text{ GHz}$	dBm	-2	0	
	@ $f_{\text{out}} = 2.5\text{ GHz}$	dBm	-2.5	-0.5	
	@ $f_{\text{out}} = 5\text{ GHz}$	dBm	-4.0	-2.0	
$ V_{\text{out(p-p)}} $	@ $f_{\text{out}} < 1\text{ GHz}$	volts	0.39	0.5	
	@ $f_{\text{out}} = 2.5\text{ GHz}$	volts	0.37	0.47	
	@ $f_{\text{out}} = 5\text{ GHz}$	volts	0.31	0.39	
P_{Spitback}	f_{out} power level appearing at RFin or $\overline{\text{RFin}}$ (@ $f_{\text{in}} = 12\text{ GHz}$, Unused RFout or $\overline{\text{RFout}}$ unterminated)	dBm		-57	
	f_{out} power level appearing at RFin or $\overline{\text{RFin}}$ (@ $f_{\text{in}} = 12\text{ GHz}$, Both RFout & $\overline{\text{RFout}}$ terminated)	dBm		-77	
P_{feedthru}	Power level of f_{in} appearing at RFout or $\overline{\text{RFout}}$ (@ $f_{\text{in}} = 12\text{ GHz}$, $P_{\text{in}} = 0\text{ dBm}$, Referred to $P_{\text{in}}(f_{\text{in}})$)	dBc		-30	
H_2	Second harmonic distortion output level (@ $f_{\text{out}} = 3.0\text{ GHz}$, Referred to $P_{\text{out}}(f_{\text{out}})$)	dBc		-30	

Notes:

- $V_{\text{PwrSel}} = V_{\text{EE}}$.
- $V_{\text{PwrSel}} = \text{Open Circuit}$.

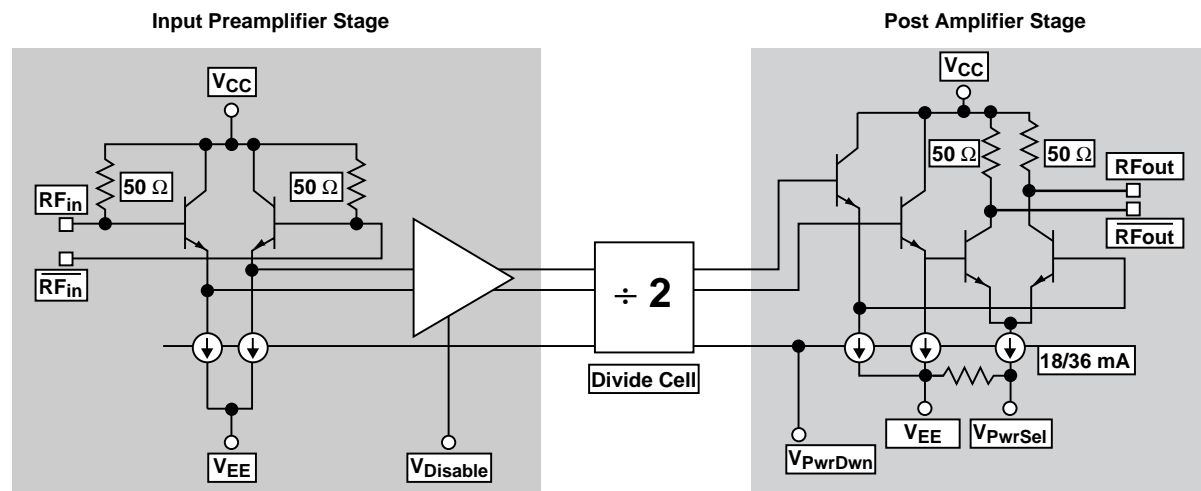


Figure 1. HMMC-3002 Simplified Schematic.

Applications

The HMMC-3002 is designed for use in high frequency communications, microwave instrumentation and EW radar systems where low phase-noise PLL control circuitry or broad-band frequency translation is required.

Operation

The device is designed to operate when driven with either a single-ended or differential sinusoidal input signal over a 200 MHz to 16 GHz bandwidth. Below 200 MHz the prescaler input is “slew-rate” limited requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to DC when driven with a square-wave. AC coupling at the RFin pad is recommended for most applications.

The device can be operated from either a single positive or single negative supply. For positive supply operation V_{CC} is nominally biased at any voltage in the +4.5 to +6.5 volt range with V_{EE} (or V_{EE} & V_{PwrSel}) grounded. For negative bias operation V_{CC} is typically grounded and a negative

voltage between -4.5 to -6.5 volts is applied to V_{PwrSel} (or V_{EE} & V_{PwrSel}).

Several features are designed into this prescaler:

1) Dual-Output Power Feature

Bonding both V_{EE} and V_{PwrSel} pads to either ground (positive bias mode) or the negative supply (negative bias mode), will deliver ~6.0 dBm [0.99 V_{p-p}] at the RF output port while drawing ~80 mA supply current. Eliminating the V_{PwrSel} connection results in reduced output power and voltage swing, 0 dBm [0.5 V_{p-p}] but at a reduced current draw of ~60 mA resulting in less overall power dissipation. (NOTE: V_{EE} must ALWAYS be bonded and V_{PwrSel} must NEVER be biased to any potential other than V_{EE} or open-circuited.)

2) V_{Logic} ECL Contact Pad

Under normal conditions no connection or external bias is required to this pad and it is self-biased to the on-chip ECL logic threshold voltage ($V_{CC} - 1.35$ V). The user can provide an external bias to this pad (1.5 to 1.2 volts

less than V_{CC}) to force the prescaler to operate at a system generated logic threshold voltage.

3) Input Disable Feature

By applying an external bias to this contact pad (more positive than $V_{CC} - 1.35$ V), the input preamplifier stage is locked into either logic “high” or logic “low” preventing frequency division and any self-oscillation frequency which may be present.

4) Prescaler Power-Down

By applying an external bias to this contact pad (more positive than $V_{EE} + 3.2$ V), the supply current can be reduced to ~5 mA also preventing frequency division and any self-oscillation frequency which may be present while decreasing the power dissipation to ~zero.

5) Input DC Offset

Another method used to prevent false triggers or self-oscillation conditions is to apply a 20 to 100 mV DC offset voltage between the RFin and \overline{RFin} ports. This prevents noise or spurious low level signals from triggering the divider.

Optional DC Operating Values/Logic Levels ($T_A = 25^\circ\text{C}$)

Function	Symbol	Conditions	Min. (volts/mA)	Typical (volts/mA)	Max. (volts/mA)
Logic Threshold ^[1]	V_{Logic}		$V_{CC} - 1.5$	$V_{CC} - 1.35$	$V_{CC} - 1.2$
Input Disable	$V_{Disable(High)}$ [Disable]		$V_{Logic} + 0.25$	V_{Logic}	V_{CC}
	$V_{Disable(Low)}$ [Enable]		V_{EE}		$V_{Logic} - 0.25$
	$I_{Disable}$	$V_D > V_{EE} + 3$ $V_D < V_{EE} + 3$	$(V_{Disable} - V_{EE} - 3) / 500$ 0		
Prescaler Power-Down	$V_{PwrDwn(High)}$ [Power-Down]		$V_{EE} + 3.9$	$V_{EE} + 3.2$	V_{CC}
	$V_{PwrDwn(Low)}$ [Power-Up]		V_{EE}		$V_{EE} + 2.7$
	I_{PwrDwn}	$V_P > V_{EE} + 2.7$ $V_P < V_{EE} + 2.7$	$(V_{PwrDwn} - V_{EE} - 3) / 500$ 0		

Note:

1. Acceptable voltage range when applied from external source.

Assembly Techniques

Figure 3 shows the chip assembly diagram for single-ended I/O operation through 16 GHz. For positive supply operation, V_{CC} is typically biased to a positive voltage between +4.5 and +6.5 volts and V_{EE} is grounded. For negative supply operation, V_{EE} is typically biased between -4.5 to -6.5 volts and V_{CC} is grounded. In either case the supply contact to the chip must be capacitively bypassed to provide good input sensitivity and low input power feedthrough. All bonds between the device and this bypass capacitor should be as short as possible to limit the inductance. For operation at frequencies below 1 GHz, a large value capacitor must be added to provide proper RF bypassing.

To aid in providing higher frequency bypassing a special $V_{CC(Bypass)}$ pad has been added to the chip and must be tied to RF ground.

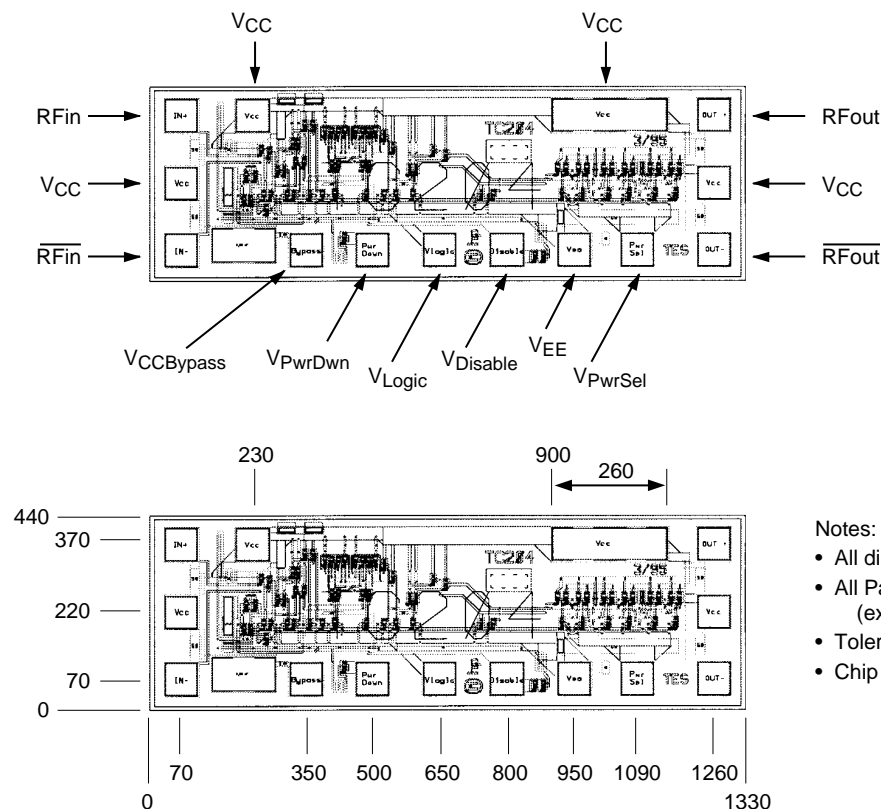
In general, AC coupling capacitors are recommended on the RFin and RFout connections to the device. For negative supply operation the AC coupling cap is not critical since V_{CC} is typically grounded and the DC voltage present on RFin/RFout is ~ 0 volts. For positive supply operation, V_{CC} is positively biased resulting in a positive DC voltage appearing at RFin or RFout. In this case a AC coupling cap is required.

Due to on-chip $50\ \Omega$ matching resistors at all four RF ports, no external termination is required.

However, improved “Spitback” performance (~ 20 dB) and input sensitivity can be achieved by terminating the unused RFout port to V_{CC} through $50\ \Omega$ (positive supply) or to ground via a $50\ \Omega$ termination (negative supply operation).

For proper handling, die-attach and electrical interconnection techniques of ESD sensitive components see HP application note #999, “GaAs MMIC Assembly and Handling Guidelines.”

GaAs MMICs are ESD sensitive. Proper precautions should be used when handling these devices.

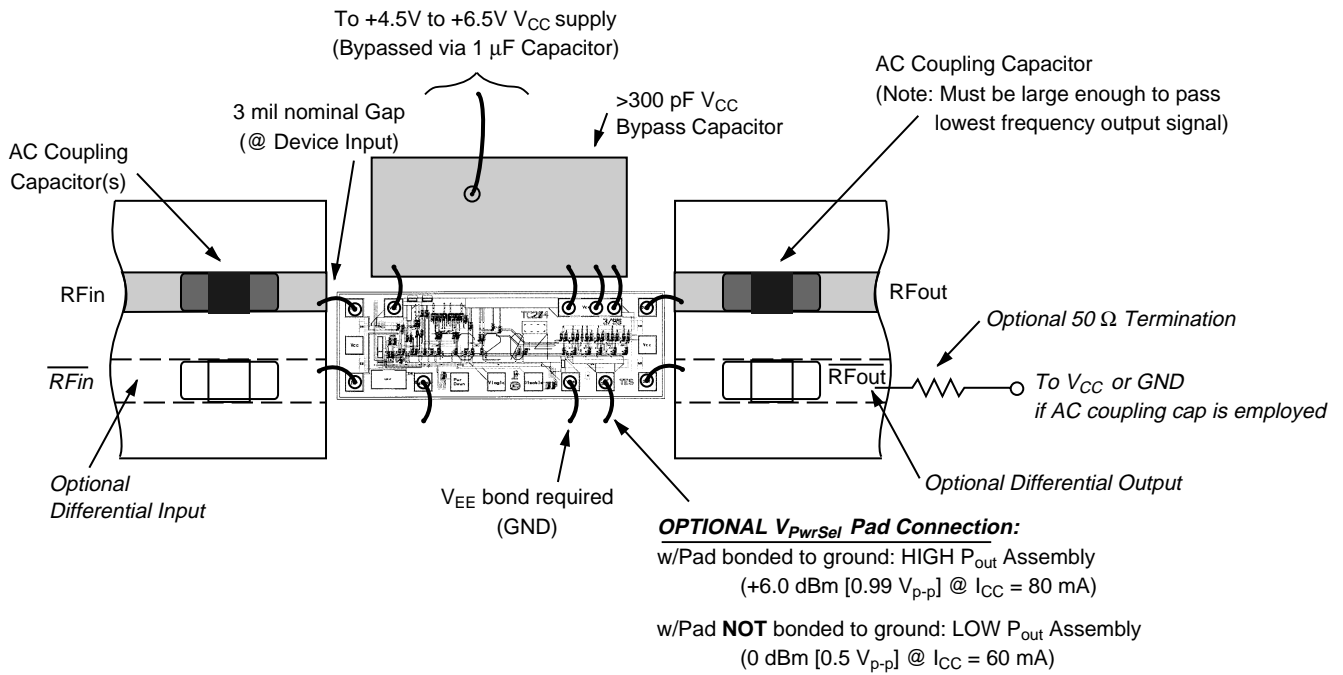


Notes:

- All dimensions in microns.
- All Pad Dim: $70 \times 70\ \mu\text{m}$ (except where noted)
- Tolerances: $\pm 10\ \mu\text{m}$
- Chip Thickness: $127 \pm 15\ \mu\text{m}$

Figure 2. HMMC-3002 Pad Locations and Chip Dimensions.

POSITIVE SUPPLY



NEGATIVE SUPPLY

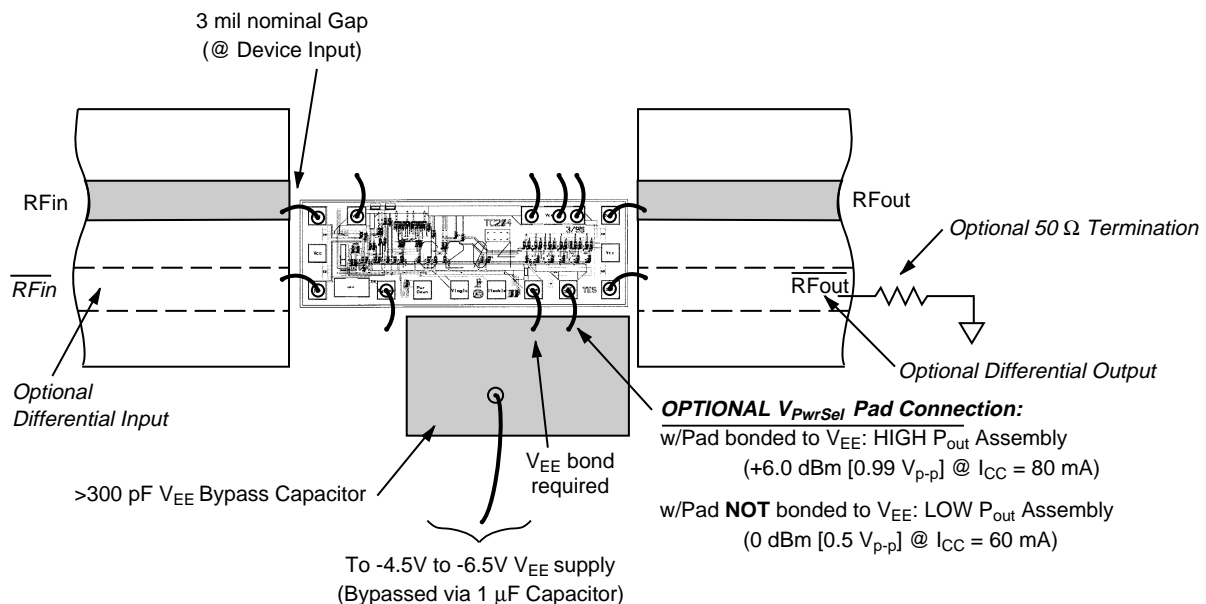


Figure 3. HMMC-3002 Assembly Diagrams.

HMMC-3002 Supplemental Data

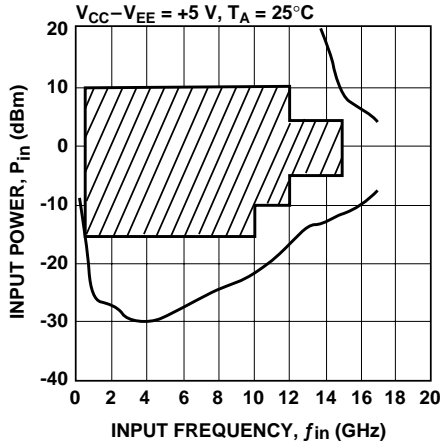


Figure 4. Typical HMMC-3002/3004/3008 Input Sensitivity Window.

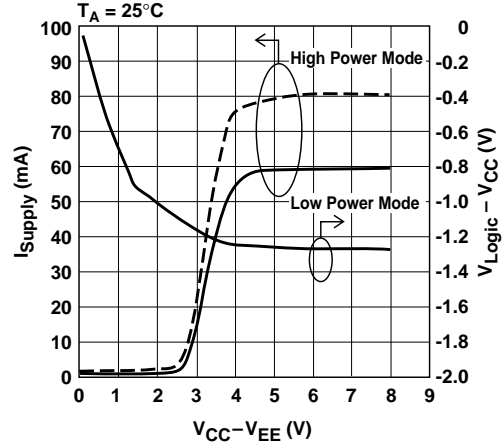


Figure 5. Typical Supply Current & V_{Logic} vs. Supply Voltage.

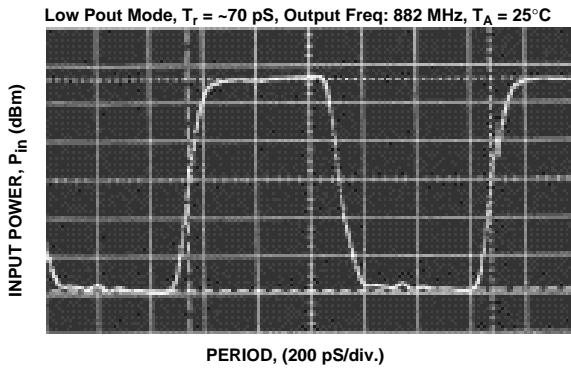


Figure 6. Typical HMMC-3002/3004/3008 Output Voltage Waveform.

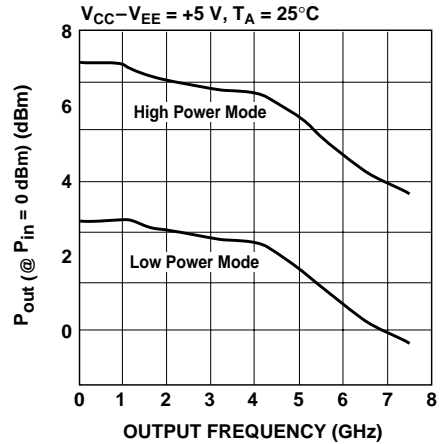


Figure 7. Typical Output Power vs. Output Frequency, f_{out} (GHz).

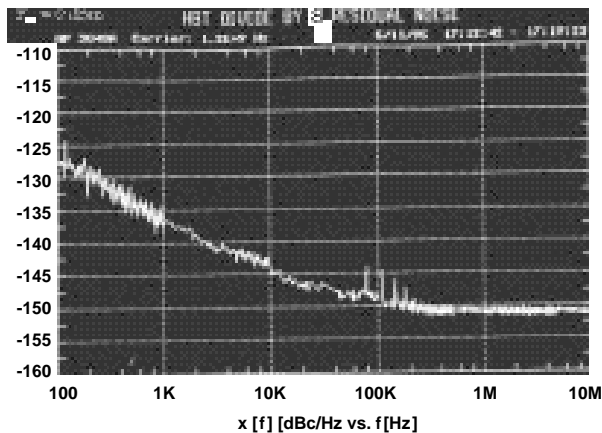


Figure 8. Typical HMMC-3002/3004/3008 Phase Noise Performance.

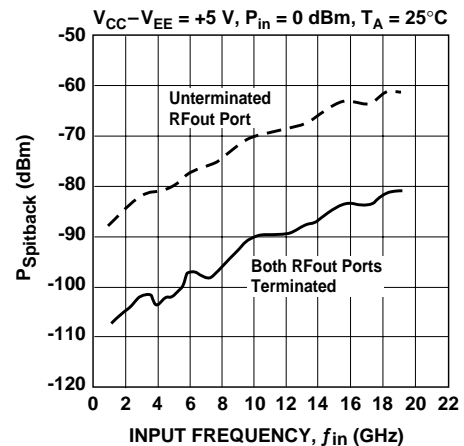


Figure 9. Typical HMMC-3002/3004/3008 "Spitback" Power. $P(f_{out})$ appearing at RF input port.

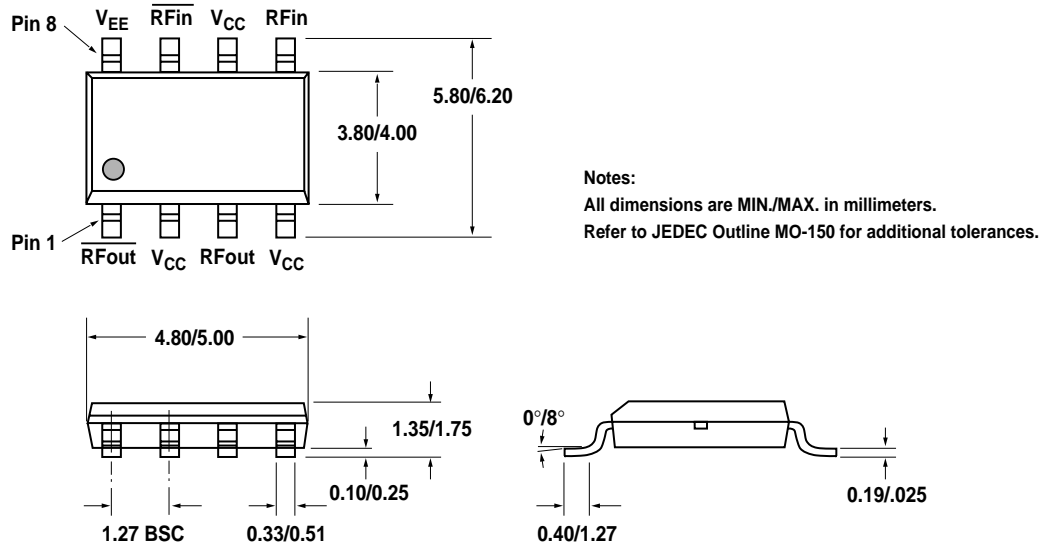


Figure 10. HMMC-3002 Package and Dimensions. (Available in near future.)

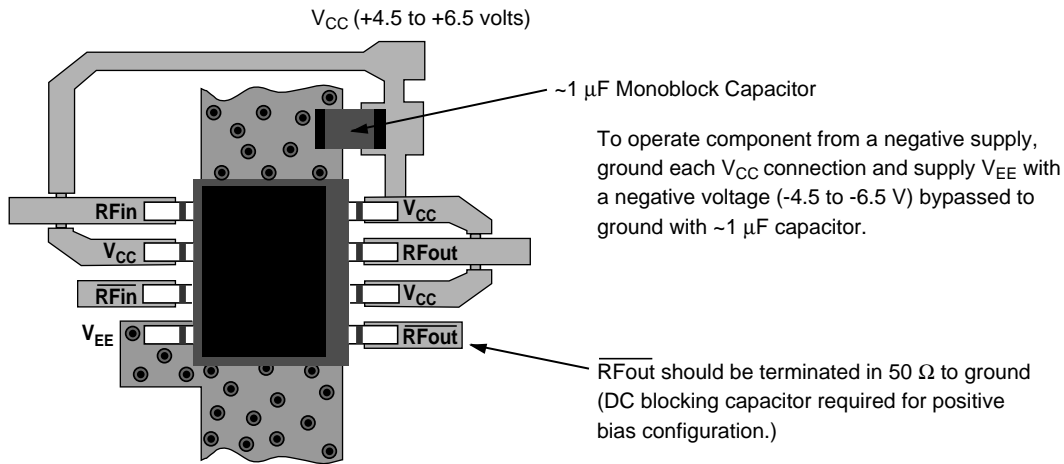


Figure 11. HMMC-3002 Assembly Diagram.
(Single-supply, positive-bias configuration shown)

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