Transistor Chip Use

Application Note A005

Part I. Assembly Considerations

1.0 Chip Packaging for Shipment

1.1 General

Hewlett-Packard transistor chips are shipped in chip carriers with a clear or black elastomer as a carrier medium. There are up to 100 chips in each pack. One of the corners of the pack is beveled to provide orientation for chip selection.

1.2 Opening/inspection

Chip carriers should be opened only at a clean, well-lighted station without fast-moving air. A white working surface is recommended for best visibility. The chips are kept in place by the surface tension of the elastomer on which they are placed. Once the clamps have been removed, the pack should be set down on the surface and the lid removed. Then, the paper can slowly (to avoid static-electricity generation) be lifted off the lower half. Occasionally a chip may work loose from the surface of the elastomer and turn upside down. If this happens, the chip should be carefully picked up with tweezers, turned over, and placed back on the elastomer. At this point the die can be counted or visually inspected. The reverse of the procedure outlined above should be used to close the waffle pack prior to storage or die attach operations.

1.3 Long Term Storage

Die that will be stored for long periods of time (greater than 1 – 2 weeks) should be kept in a dry nitrogen atmosphere for optimum performance and reliability. The gold-based metal systems of all Hewlett-Packard transistors are very resistant to deterioration, but the best practice is to store them in an inert atmosphere.

2.0 Handling Chips with Tweezers

Unfortunately, both silicon and GaAs materials are quite brittle (GaAs is more so) and the sharp edges of the transistor chips are easily damaged if too much pressure is applied with tweezers. A good precaution is to use only the sharpest possible tweezers with good point alignment to handle transistor chips. New operators should practice with bonding samples, which HP generally can supply free of charge.

3.0 Die Attach Procedure

Different die attach procedures are used for silicon chips and GaAs devices. To die attach a silicon chip, the chip and mounting surface are heated sufficiently for the gold of the mounting surface to mix with the gold backside of the chip and melt into the silicon of the chip, forming a gold-silicon eutectic bond. This technique is suitable because silicon can tolerate the relatively high temperatures needed for eutectic formation without endangering the silicon device.

GaAs devices are more temperature sensitive, and use instead a lower temperature gold alloy "solderdown" technique. In both cases the die-attach station should have the actual die attach area flooded with an inert (forming gas or nitrogen) atmosphere.

3.1 Silicon Bipolar Transistor Die Attach Procedure

3.1.1 The heater block temperature should be 410°C ±10°.

3.1.2 Place the circuit or package into which the transistor or capacitor will be attached on the heater block. Allow sufficient time to heat thoroughly (5 to 15 seconds depending on thermal mass).

3.1.3 Pick up a chip with tweezers (*EREM* type 5 SA recommended) and orient it properly prior to placement on the heated surface.

3.1.4 Place the chip on the heated surface and scrub with a back-and-forth motion, being careful not to scratch the top surface of the chip. Continue this until wetting occurs; this should take place within three to four scrubs.

3.1.5 If wetting does not occur check that the heater block temperature is correct and that the inert atmosphere blanket is present.

3.1.6 When wetting occurs, perform a circular scrub for one stroke to insure wetting of the chip perimeter. Carefully remove the tweezers from the die.

3.1.7 Remove the circuit or package from the heated surface and allow it to cool in air.

3.2 GaAs FET Attach Procedure

3.2.1 The heater block temperature should be 300°C ±10°.

3.2.2 Place the circuit or package into which the transistor will be attached on the heater block. Allow sufficient time to heat thoroughly (5 to 15 seconds depending on thermal mass).

3.2.3 Pick up a Au-Sn (gold-tin) preform and place it on the circuit/package in the die attach location. Use a sufficient quantity to insure good wetting and to produce a fillet around the chip.

3.2.4 Pick up a chip with tweezers (*EREM* type 5 SA recommended) and orient it properly prior to placement on the heated surface.

3.2.5 Place the chip on the heated surface and scrub with a back-and-forth motion being careful not to scratch the top surface of the chip. Continue this until wetting occurs; this should take place within 3 to 4 scrubs.

3.2.6 If wetting does not occur check that the heater block temperature is correct and that the inert atmosphere blanket is present.

3.2.7 When wetting occurs, perform a circular scrub for one stroke to insure wetting of the chip perimeter. Carefully remove the tweezers from the die.

3.2.8 Remove the circuit or package from the heated surface and allow it to cool in air.

4.0 Bonding Procedures

Either gold-ball bonding or thermocompression (wedge) bonding may be used on almost all HP transistors. Bonding pad sizes and metal adhesion strengths are compatible with either technique, thus giving the circuit designer the flexibility to use either approach. In general, for higher frequency use (greater than 8 GHz), a thermocompression wedge bond is preferred because of the resulting shorter bond lengths and reduced electrical parasitics.

4.1 Ball Bonding

HP, in the majority of cases, has used *West Bond* Model 7700 (Thermosonic) and 7716 (Thermocompression) series ball bonders for assembly, but any bonder capable of handling 0.001" or smaller diameter gold wire is appropriate. Prestressed (annealed) wire is preferred. Two modes of operation, Thermosonic and Thermocompression, are possible, with slightly different conditions required for each.

4.1.1 Heater Block Temperature

4.1.1.1 Thermocompression

Calibrate the heater block temperature to 300°C ± 10° for Si Bipolar devices and 260°C ±10° for GaAs FETs.

4.1.1.2 Thermosonic (or Ultrasonic)

Calibrate the heater block temperature to 150°C ± 10°.

4.1.2 Calibrate bond force as follows:

Ball Bond:	0.0007, 15-20 gram	MWB:	0.0007, 20 ±2
	0.001, 20-30 gram		0.001, 25 ±2

4.1.3 Proceed with bonding according to machine specifications.

4.1.4 General Comments:

The normal approach is to place the ball on the circuit bonding pad and then complete the second bond to the chip.

4.2 Thermocompression Wedge Bonding

In circuits where there is good access to the transistor chip bonding pads and to the circuit elements to which the chip bonds run, a variety of wedge bonders, including many new semi-automatic units, can be used. In situations where horizontal access is very limited (such as a transistor package), a manual machine with a small chisel wedge may be the most appropriate. The wedge does not have to be heated, but if it is the heater block temperature may be lowered slightly as specified in the next section. Since the exact amount of temperature adjustment required will vary from machine to machine, establishing the final temperature is an empirical process.

4.2.1 Wedge Bonding Procedure

4.2.1.1 Set the heater block to 300°C ±10° for Si Bipolar transistors and 260°C ±10° for GaAs FETs.

4.2.1.2 Wire diameters of 0.0005" to 0.001" are used most often, and the wire should be prestressed (annealed).

4.2.1.3 Always make the bonds from the circuit element to the transistor bonding pads to minimize pad damage. Also, bonds should be made to the source and drain pads of an FET prior to making the bond to the gate pad. This minimizes the potential for electrostatic discharge damage (see section 6.0).

4.2.1.4 Tip bonding pressure should be approximately 15 – 20 grams and should not exceed 20 grams. A good rule of thumb is that the "footprint" of the wedge on the gold wire should be about two wire diameters across (minimum of 1.5 and maximum of 2.5 diameters) for a good bond.

5.0 Material:

Vendor:	MWS
Wire:	0.0007 mil, P/N 453-18496, EL 1-3%
Vendor:	HYDROSTATICS INC.
Wire:	0.001 mil, P/N 453-010977-001, EL 3-8%
Vendor:	DEWEYL TOOL
Bonding Wedge:	K-1/16-L-60-F1507-T1
Vendor:	GAISER
Bonding Caps:	1/8", P/N 1251-15-35, (3-4-3) 1/16", P/N 1551-15-375P-39 (3-5-5)
Vendor:	SEMI ALLOYS
Preforms:	0.6, P/N 10902-5
Vendor:	WILLIAMS PRECIOUS METALS
Preforms:	0.8, P/N 855-010982-006

6.0 Electrostatic Discharge Precautions

The following discussion applies mainly to GaAs FET devices, but excess voltages can damage a silicon bipolar device as well. Slight degradation of a GaAs FET device can occur with electrostatic potentials as low as 500 volts and capacitances on the order of that of the human body. Unfortunately, it is very easy to generate static charge of this magnitude through the motion of an arm, by sliding plastic objects together, or by the motion of the body on a chair cushion. Static discharges that we can feel or hear are on the order of 10 kV by comparison.

Any time a potential difference can be applied between the elements of a transistor, damage can result. Therefore, in chip form, prior to bonding, the transistor is relatively immune to damage. Once the bonding has been started though, caution must be exercised to prevent device damage. HP uses the following procedures for E.S.D. prevention in assembly areas, and recommends their use.

1. Operators use wrist straps connected to earth ground through 1 megohm resistors (for operator safety).
2. All equipment is grounded to earth ground including heater blocks, bonders, and test equipment.
3. Work surfaces are covered with anti-static mats (not metal) which are grounded to earth ground.
4. All operators wear anti-static smocks made of material which is woven with 1% stainless steel wire.
5. Floors and seat cushions are treated periodically with an anti-static solution.
6. A periodic survey of work areas is conducted with a static potential meter to monitor potential build-ups or grounding failures.

Part II. Design Considerations

1.0 RF Performance Considerations

1.1 General

In general, optimum chip transistor performance is obtained with the shortest possible bond wire lengths. This puts obvious constraints on circuit layout and chip positioning. Most designers using FETs minimize gate and source bond lengths at the expense of longer drain bond wires. Thermocompression-wedge bonding yields the shortest bond wire length for a given pad separation because the bond comes off the pad in a more horizontal direction.

1.2 Hewlett-Packard Chip Device Characterization

HP GaAs FET chip transistors are characterized on a standard chip carrier which consists of 50 ohm alumina microstrip lines (of 0.100 inch length and 0.025 inch thickness) on either side of a metal bar (0.030 inch long) upon which the FET chip is mounted. The transistor is centered on the bar and bond wires for input (gate) and output (drain) are of equal length. Minimum bond lengths for the sources are

used. The S-parameter data, as presented in HP chip transistor data sheets, includes the bond wire inductance (approximately 0.7 nH per wire), microstrip line end-effect capacitance (about 0.02 pF) and microstrip line losses (about 0.1 dB). A designer modeling the chip should adjust these parasitic elements appropriately for the specific circuit configuration.

Bipolar transistor chips are characterized in a slightly different configuration because the substrate/backside of the chip is the collector and the chip is mounted on the output 50 ohm line. The emitter pad (or multiple pads, if used) is bonded to ground via holes through the alumina substrate and the base is connected to the input line. Again, bond inductances (about 0.5 nH base and 0.2 nH emitter), end-effect capacitances (about 0.02 pF) and 0.025" alumina microstrip losses (about 0.1 dB) are included in the chip data.

2.0 Heatsink Material Considerations

Although a detailed evaluation of device heatsinking is beyond the scope of this application note, some comments on the topic are in order. In general, for small signal devices the DC power dissipation levels are low enough that the heatsink material is relatively unimportant. As device dissipation levels approach 250 milliwatts and operating temperatures increase, a higher thermal conductivity material is needed for the chip mounting surface. The best choices, given fabrication constraints for a particular circuit, are gold plated copper or gold plated beryllium oxide (BeO).

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Data Subject to Change

Obsoletes 5091-8802E

5968-3242E (1/99)