1800 MHz Medium Power Amplifier using the HBFP-0450 Silicon Bipolar Transistor

Application Note 1168

Introduction

Hewlett-Packard's HBFP-0450 is a high performance, medium power Isolated Collector transistor housed in a 4-lead SOT-343 (SC-70) surface mount package. Described as a high performance, medium power, low noise transistor, the HBFP-0450 offers +19 dBm typical P-1dB at 1,800 MHz when powered from a 3 V, 50 mA supply. This amplifier design example is for use on 0.031-inch (0.8 mm) thickness FR-4 printed circuit board material. The HBFP-0450 amplifier described in this note is biased at a V_{CE} of 3 V and I_C of 50 mA and can provide a P-1dB of 18 dBm, IP3 (out) of +31 dBm, with a stable gain of 13 dB. A trade-off in power has been taken to improve the input and output return loss to better than -12 dB and to ensure unconditional stability across the entire s-parameter range (100 MHz to 10 GHz).

HBFP-0450 Medium Power Amplifier Design

Using Hewlett-Packard EESOF ADS software, a single stage amplifier was designed to provide a nominal 18 dBm output P1dB, IP3 (out) performance better than 30 dBm with greater than 13 dB of small signal stable gain with the device being operated at 3 V, 50 mA.

The completed amplifier design showing component placement is shown in Figure 1.

Biasing Considerations

Typical power supply voltage in the design (V_{CC}) is 5 V, although the collector bias resistor (R3) and I_C control this value. By implementing a high delta between V_{CC} and V_{CE}, a good bias point stability over temperature can be ensured. The amplifier schematic is shown in Figure 2. Further stability over temperature and hfe variation can be achieved by taking the V_{be} source from the junction of L3 and R3, rather than directly from the voltage source.

In high volume applications Hewlett-Packard would normally recommend the use of an active bias scheme as shown in Figure 3. The active bias would assure a relatively constant bias point regardless of any changes in dc parameters from device to device. This demo board

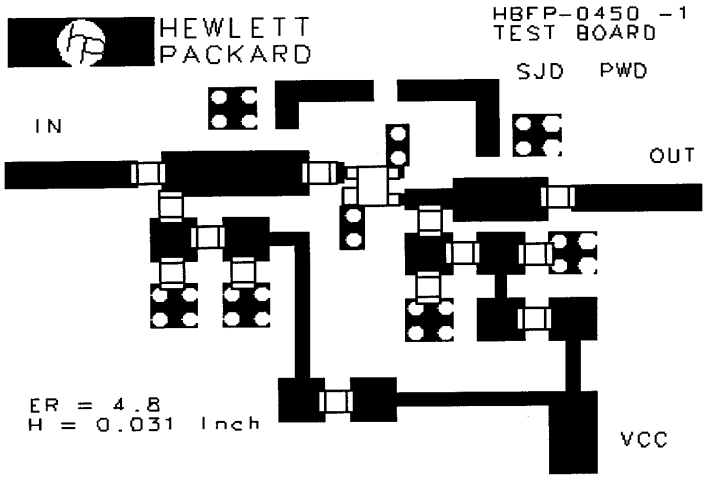


Figure 1. Board Layout with Component Placement (approx. 3X actual size)

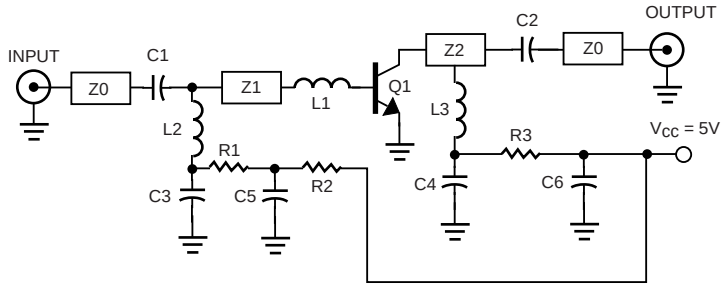


Figure 2. Schematic Diagram

uses passive biasing. Variation in hfe can be compensated by making changes to Rb (R1+R2) to ensure that the correct bias point (V_{CE}, I_C) is selected. While the biasing resistors may be chosen to ensure the correct bias point, they also aid with low frequency stability of the amplifier design. If R2 is removed, and V_{be} is offered directly from a voltage supply, there could be potential problems with low frequency stability. To alleviate this problem additional de-coupling and low frequency termination would be required. When considering higher bias voltages, the value of R2 will increase. Increasing the value of R2 above approximately 100 Ohms can compromise the low frequency stability of this design. To compensate for this, R2 should be kept low, and a second resistor can be used between C6 and the supply to set the desired bias levels.

For help on designing passive bias schemes, please refer to Hewlett-Packard's AppCad Freeware.

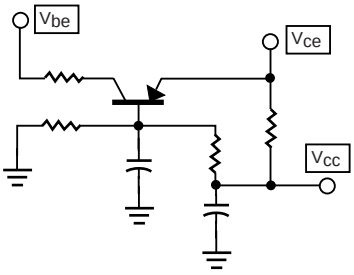


Figure 3. Active Bias Scheme

Circuit Design

The input impedance matching network is relatively straightforward. As the concern is with amplifier gain and output power, the input circuit is used to conjugately match from 50 Ohms directly to the base of the transistor. To achieve this the matching network is built using a

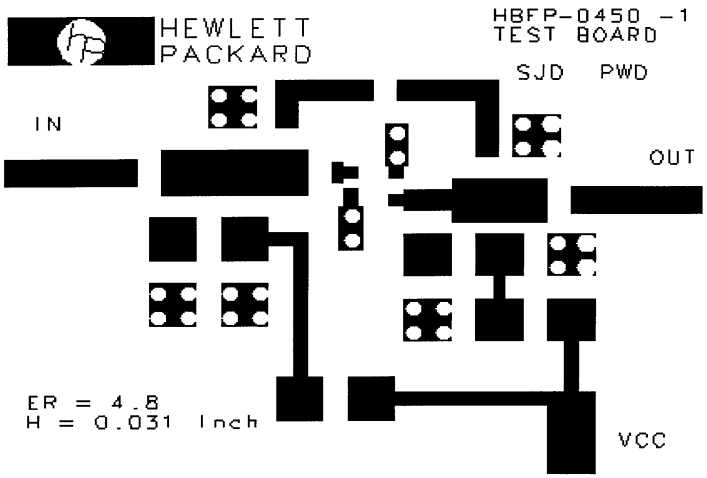


Figure 4. Demonstration Board Layout (approx. 3X actual size)

series capacitor (C1), series microstrip line (Z1), and a series inductor (L1). C1 provides DC blocking and low frequency roll-off, while Z1 is used to match directly to the base of the transistor. L1 has been included to allow some tuning flexibility on the demo board.

The base current is injected via the shunt inductor L2. C3, R1, and C5 will produce a low frequency resistive termination, while providing the necessary bias decoupling. R2 is used to set the transistor's base current, and therefore operating point (I_C = hfe.Ib). See Biasing Considerations for further details of R2 selection.

The output impedance match is performed using a series capacitor (C2), a series microstrip line (Z2), and a shunt inductor (L3) that doubles as an injection source for the collector current. To ensure the highest possible output power, while maintaining unconditional stability, no collector-resistive-loading has been used. The output matching components are selected to optimize the trade-off between output power and S22. The optimum component selection was determined by the combination of linear and non-linear simulation in addition to confirmation on the bench. C4, R3, and C6 provide bias decoupling with a good low frequency termination.

The selected component values are shown in Tables 1 and 2.

Circuit Simulation

Using Hewlett-Packard's EESOF ADS software the amplifier circuit can be simulated in both linear and non-linear modes of operation. Figure 13 shows the schematic layout from ADS (Linear Simulation). When preparing the initial design it is very important to use supplier component models rather than ideal models. This is especially true for a discrete device with high gain from a few megahertz to several gigahertz. Ideal models do not reflect Inductor SRF, component package parasitics, or the true performance of a SMT capacitor. The

Table 1. Initial Component Selection

Number	Description
C1	0.8 pF Chip Capacitor
C2	3.3 pF Chip Capacitor
C3	10 pF Chip Capacitor
C4	4.3 pF Chip Capacitor
C5, C6	1000 pF Chip Capicitor
L1	3.3 nH
L2	47 nH
L3	3.3 nH
Q1	Hewlett-Packard HBFP-0450 Silicon Bipolar Transistor
R1	50 Ohm chip Resistor
R2	6.9K Ohm chip Resistor. Used to set IC
R3	40 Ohm Chip Resistor
Z0	50 Ohm Microstrip Line
Z1, Z2	Microstrip Matching Network

Table 2. Alternative Component Selection

Number	Description
C1	0.8 pF Chip Capacitor
C2	3.3 pF Chip Capacitor
C3	10 pF Chip Capacitor
C4	4.3 pF Chip Capacitor
C5, C6	1000 pF Chip Capicitor
L1	3.3 nH
L2	47 nH
L3	5.6 nH
Q1	Hewlett-Packard HBFP-0450 Silicon Bipolar Transistor
R1	50 Ohm chip Resistor
R2	6.9K Ohm chip Resistor. Used to set IC
R3	40 Ohm Chip Resistor
Z0	50 Ohm Microstrip Line
Z1, Z2	Microstrip Matching Network

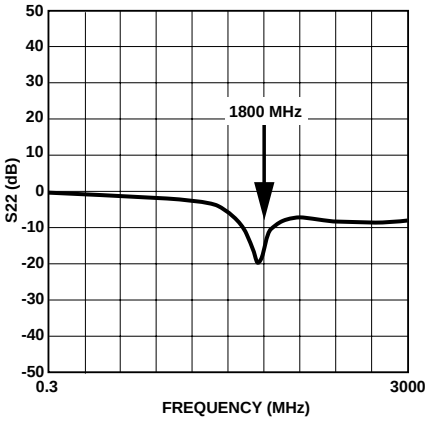


Figure 5. Initial Circuit Design S22

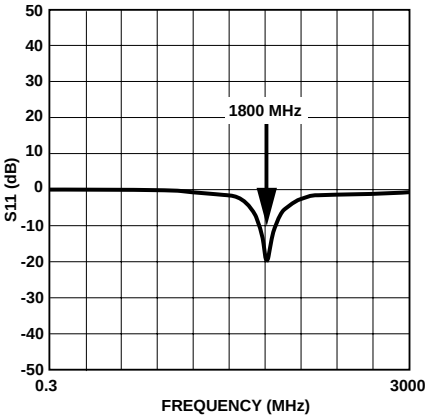


Figure 6. Initial Circuit Design S11

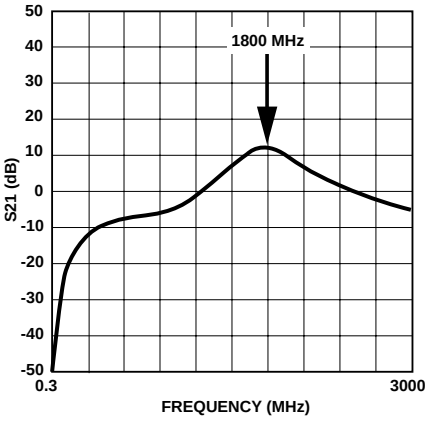


Figure 7. Initial Circuit Design S21

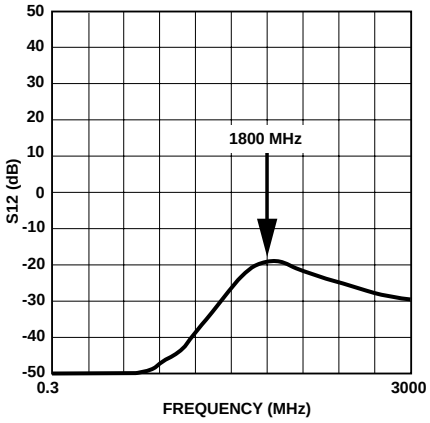


Figure 8. Initial Circuit Design S12

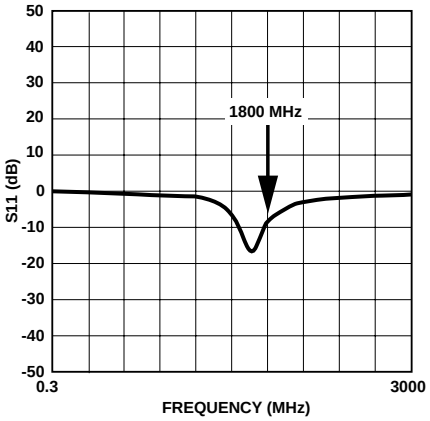


Figure 9. Alternative Design S11

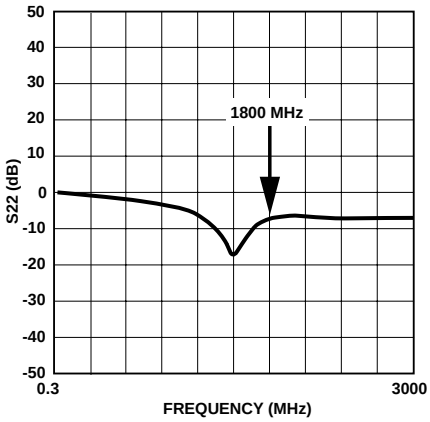


Figure 10. Alternative Design S22

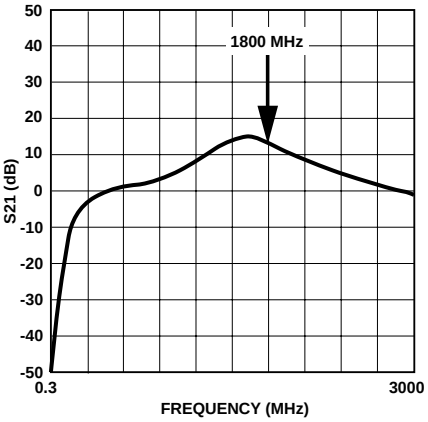


Figure 11. Alternative Design S21

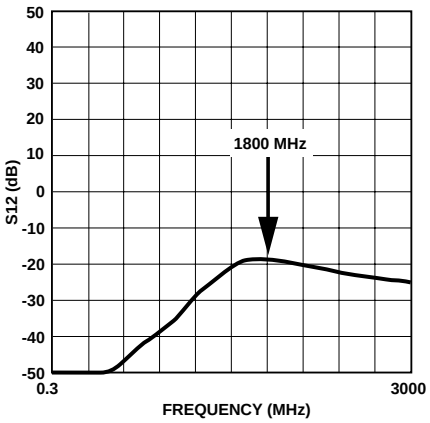


Figure 12. Alternative Design S12

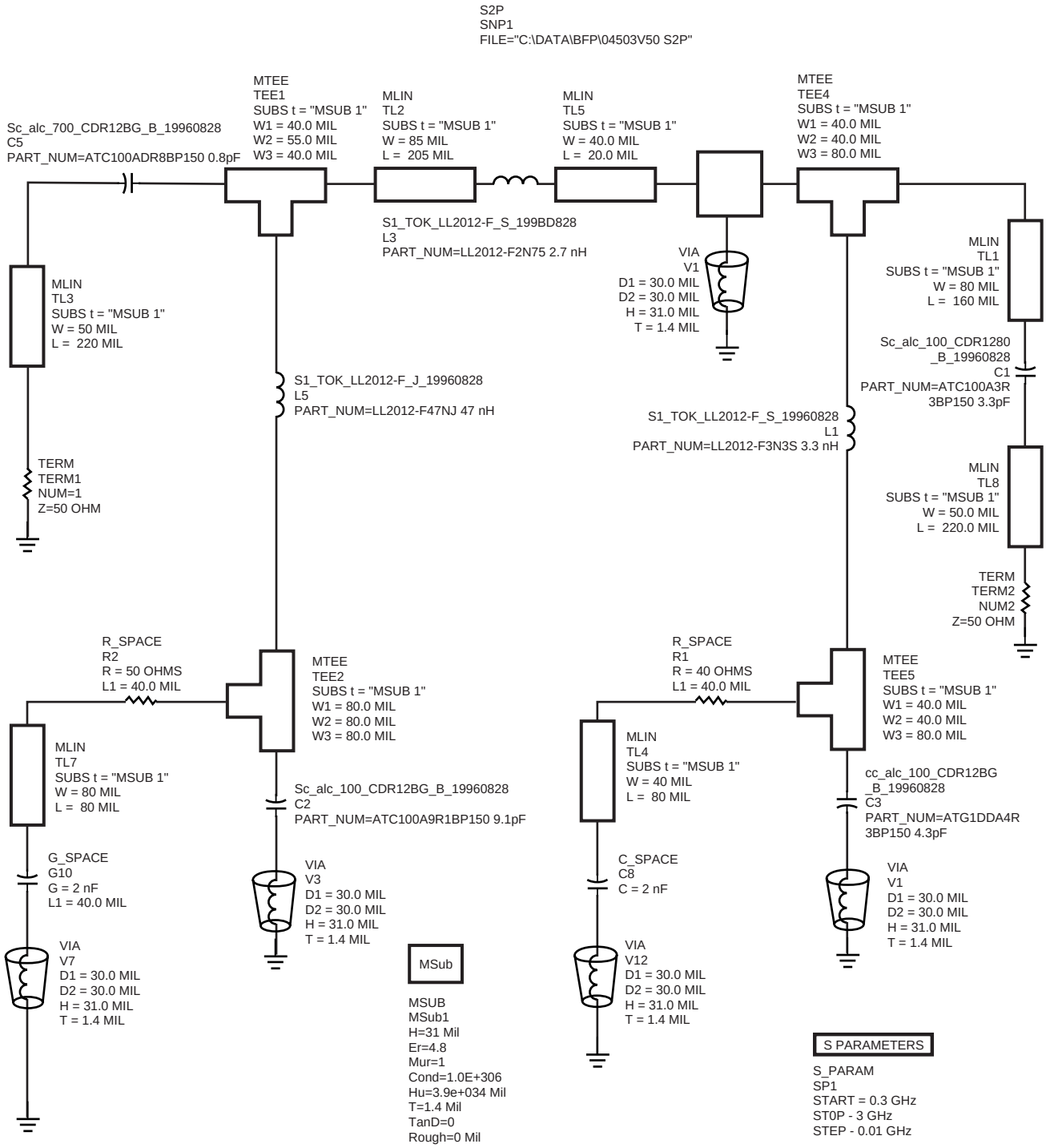


Figure 13. Schematic Layout from ADS (Linear Simulation)

non-ideal characteristics of a capacitor or inductor are negligible at low frequencies, but for applications above 100 MHz these characteristics cannot be ignored. Real capacitors will exhibit inductive and resistive impedances in addition to the capacitance, while an inductor will have capacitive and resistive impedances in addition to the inductance.

The initial design was completed using s-parameters. This provides an excellent “first estimate” for the input and output matching circuits required, but does restrict you to linear analysis. To analyze the circuit for non-linear power performance, the Harmonic Balance Simulator must be used.

Linear Analysis

The Linear S-parameter analysis was initially performed using the s-parameters given in Appendix A. Inserting these into ADS is performed by selecting the Linear Data File Palette, and highlighting the S2P: 2-Port S-parameter File. This can be seen at the center of Figure 13. Within this element the hbfp0450.s2p file can be selected. All other parameters can be left as default.

All other components can be selected from the supplier’s component library and placed as shown in Figure 13.

The s-parameter simulation controller (SP1) should be inserted into the schematic layout and set-up to simulate the design across the entire s-parameter frequency range. To enable analysis of the stability factor, K, the stabfact element must be inserted into the schematic from the s-parameter palette. Figure 13 shows the linear analysis schematic, with the s-parameter controller and stability factor element included.

Once the simulation has been completed the s-parameters for the designed circuit can be plotted in the data viewer. Figures 14 through 17 show the s-parameters for this design. It should also be noted that these plots are almost identical to those measured in Figures 5 through 8.

Figure 18 shows a plot of the stability factor K across the entire s-parameter range. K is greater than 1 across the entire plot, therefore it can be concluded that the simulated design is unconditionally stable.

Non-Linear Analysis

The circuit that is used for the non-linear analysis is almost identical to that used for linear analysis, except for the addition of the power supplies, and the s-parameter data file is replaced by the non linear transistor model shown in Appendix B. If the model is provided in SPICE format, it can be imported directly into ADS using the File-Import option. See ADS for further details on SPICE file importing.

To perform the non-linear analysis the Harmonic Balance controller, or one of the other non-linear simulators, must be inserted into the

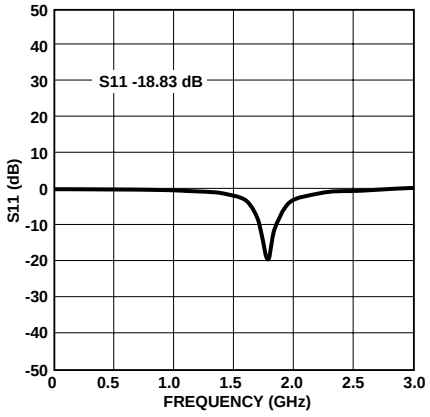


Figure 14. Simulated S11

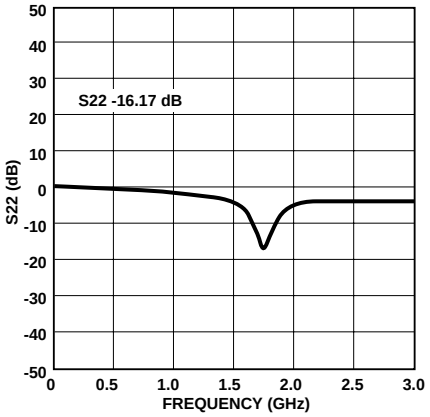


Figure 15. Simulated S22

schematic layout. The non-linear simulators can be selected from the appropriate Palette, and inserted directly into the schematic. For this example we are looking for P1dB, and IP3out performance. To achieve this we need to select the harmonic balance simulator and the XDB simulator. The setup for these simulators is shown in Figure 19.

To measure IP3out performance, the IP3out function must be inserted into the schematic. This function can be selected from the Harmonic Balance Palette. The function for IP3out looks like:

IP3out=ip3_out(vout,fundFreq,imFreq,zRef)

where:

vout is the signal voltage at the output,
fundFreq and imFreq are the harmonic frequency indices for the fundamental and intermodulation frequencies, respectively, and
zRef is the reference impedance.

In this example the exact function used is IP3out=ip3_out(vout,{1,0},{2,1},50).

Before this function will work correctly you must name the output node vout. This is the node at which IP3 level will be measured.

To simulate the P1dB performance the XDB simulator must be inserted and configured as shown in Figure 19. Once the simulation has been completed, the data can be viewed in the data viewer.

The non-linear simulated performance of this example design is very close to real-life. The s-parameters look almost identical to those shown in Figures 14 through 18, with only a slight frequency shift. This difference is due to slight differences between the measured s-parameters and those predicted by the model. For most designs this will provide adequate results. The simulated P1dB and IP3out performance is also very close to that measured on the bench. Using the component selection in Table 1, the simulator indicates a P1dB of 17.26 dBm and an IP3out of 30 dBm. Using the alternative component selection in Table 2, the simulator predicts a P1dB of 19.18 dBm and an IP3out of 30 dBm. All these predictions are within 1 dB of the tested circuit performance.

Artwork Generation

The artwork for this demo board is shown in Figure 4. The overall board size is approximately 1.2 inches (3.5 cm) by 1 inch (2.54 cm), making this a very compact design. The board material chosen for this example is 0.031-inch thickness FR-4. The artwork for this design was extracted directly from ADS using the layout generator. This can output the file in a variety of formats, all of which can be supported by board manufacturers.

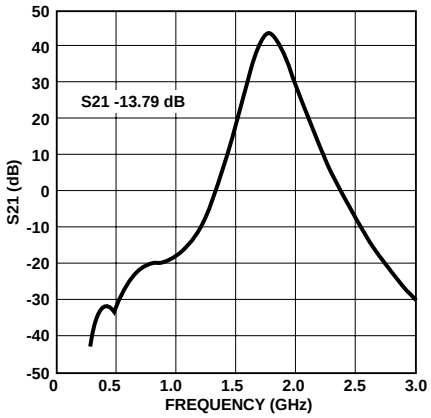


Figure 16. Simulated S21

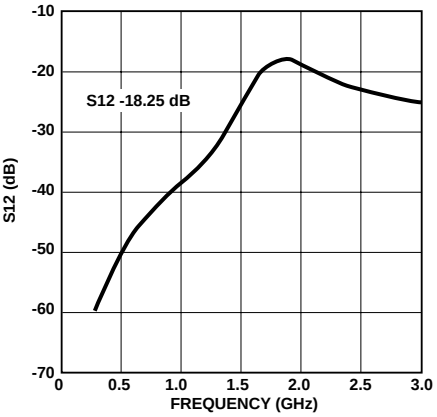


Figure 17. Simulated S21

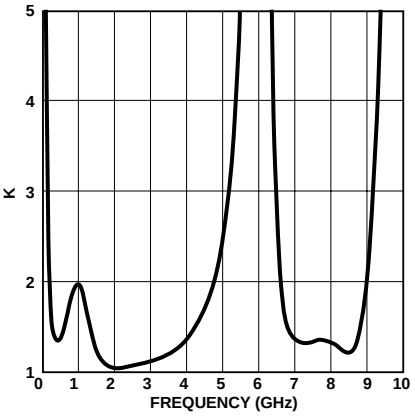


Figure 18. Simulated Stability Factor K

Test Results

Using the HBFP-0450 demo board, performance trade-off can be evaluated. Using the original component selection shown in Table 1, the performance requirements are almost met. As can be seen in Figures 5 and 6 the input (S11) and output (S22) match for this design is better than -16.5 dB in both cases, with an S21 of 12.9 dB as shown in Figure 7. The P-1dB performance of this circuit is 16.9 at 1,800 MHz, with input IP3 (out) of 31 dBm.

As this initial design did not meet the criteria for P-1dB, alternative component values were selected as per Table 2. The P-1dB and gain for this second design was higher at 18.6 dBm and 13.1 dB respectively. The gain performance can be seen in Figure 11. The IP3 performance had deteriorated to 30 dBm. To achieve this additional output power a trade-off in S11 and S22 had to be taken. This is shown in Figures 9 and 10.

To ensure that the optimum output power is being achieved from a set bias condition, load-pull tests can be performed within the ADS simulator. In reality, slight circuit alterations may be needed to compensate for component model inaccuracies.

Higher Bias Currents

Although this design has been performed for 3 V, 50 mA bias conditions, the HBFP-0450 can be driven at higher V_{CE} and I_C. To demonstrate the advantages of this the second design using the component selection in Table 2 was biased at 3 V, 70 mA. This produced a P-1dB of 20 dBm, while maintaining an IP3 of 30 dBm. Higher bias currents and collector voltages will produce higher levels of output power, but the maximum power, voltage and current ratings as specified on the data sheet for this device must not be exceeded. Attention should also be given to the overall amplifier stability when changing the value of R3 (please see biasing considerations for further details).

Conclusion

The successful design of an unconditionally stable, medium power amplifier requires a careful balance between all the required parameters. This particular design shows that the HBFP-0450 can be used to design an unconditionally stable, medium power amplifier with relatively high gain, excellent IP3 performance, while maintaining a good input and output match.

By using the non-linear model attached in Appendix A and the Hewlett-Packard ADS Simulation software, a very accurate design can be completed without the need for multiple iterations.

Harmonic Balance

HarmonicBalance
HB1
MaxOrder = 4
Freq(1) = 1.8 GHz
Freq(2) = 1.8 GHz
Order(1) = 3
Order(2) = 3

Gain Compression

XDB
HB2
MaxOrder = 4
Freq(1) = 1.8 GHz
Freq(2) = 1.8 GHz
Order(1) = 3
Order(2) = 3
GC_XdB = 1
GC_InputPort = 1
GC_OutputPort = 2
GC_InputFreq = 1.8 GHz
GC_OutputFreq = 1.8 GHz
GC_InputPowerTol = 1e-3
GC_OutputPowerTol = 1e-3
GC_MaxInputPower = 100

Figure 19. Harmonic Balance and Gain Compression

Appendix A.

hbfp0450.s2p

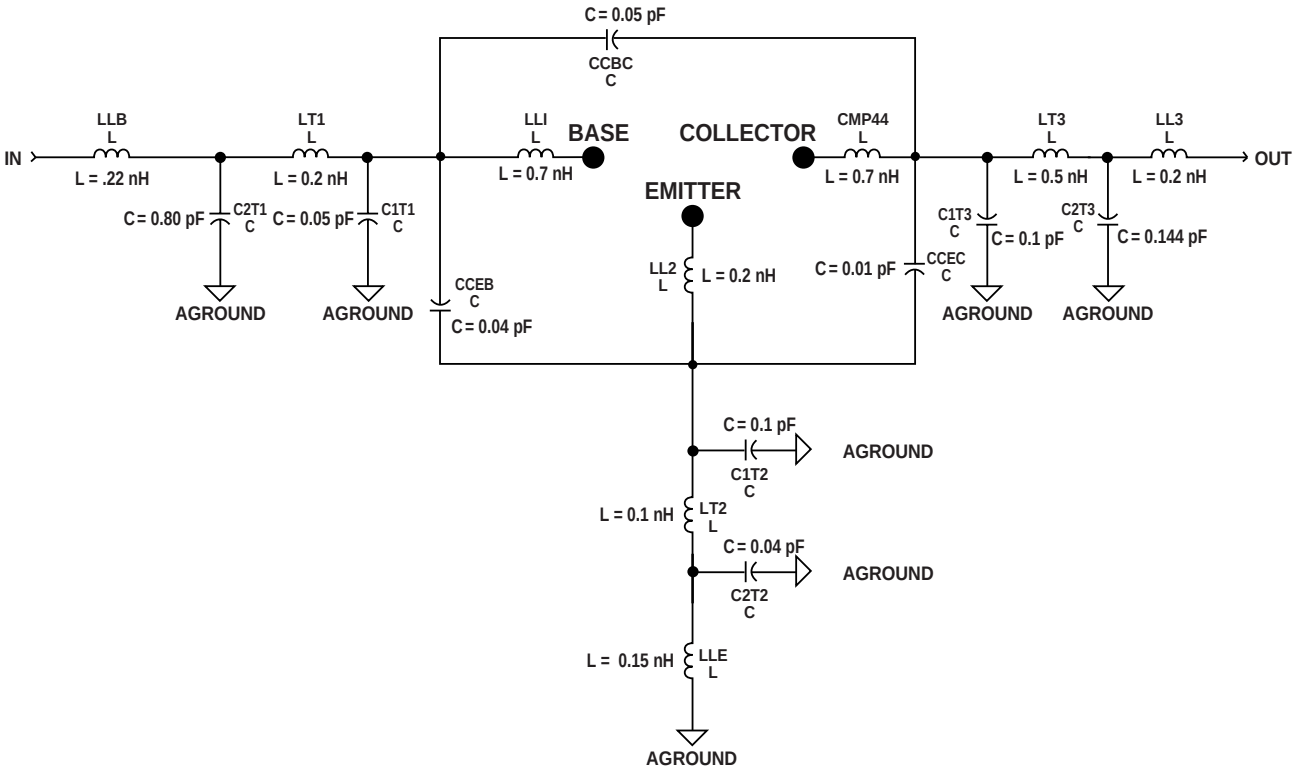
!HBFP-0450 VC=3V IC=50mA VB= 0.915 IB=570.54µA
ghz s ma r 50

0.1	0.53	-66	36.115	150	0.020	64	0.85	-39
0.5	0.66	-152	14.327	99	0.046	39	0.47	-117
0.9	0.68	-176	8.197	82	0.057	39	0.39	-147
1.0	0.68	-180	7.376	79	0.060	39	0.38	-153
1.5	0.70	165	4.879	67	0.076	40	0.36	-174
1.8	0.70	158	4.050	60	0.086	39	0.36	176
2.0	0.71	153	3.645	56	0.092	38	0.36	171
2.5	0.71	143	2.919	46	0.109	34	0.37	160
3.0	0.72	134	2.446	37	0.126	30	0.38	150
4.0	0.71	116	1.883	19	0.160	18	0.39	133
5.0	0.72	97	1.548	0	0.190	4	0.40	114
6.0	0.75	79	1.300	-19	0.212	-10	0.43	96
7.0	0.78	61	1.101	-36	0.226	-25	0.48	79
8.0	0.80	46	0.952	-52	0.237	-38	0.52	65
9.0	0.83	31	0.844	-68	0.247	-52	0.54	51
10.0	0.84	17	0.756	-83	0.254	-66	0.57	35

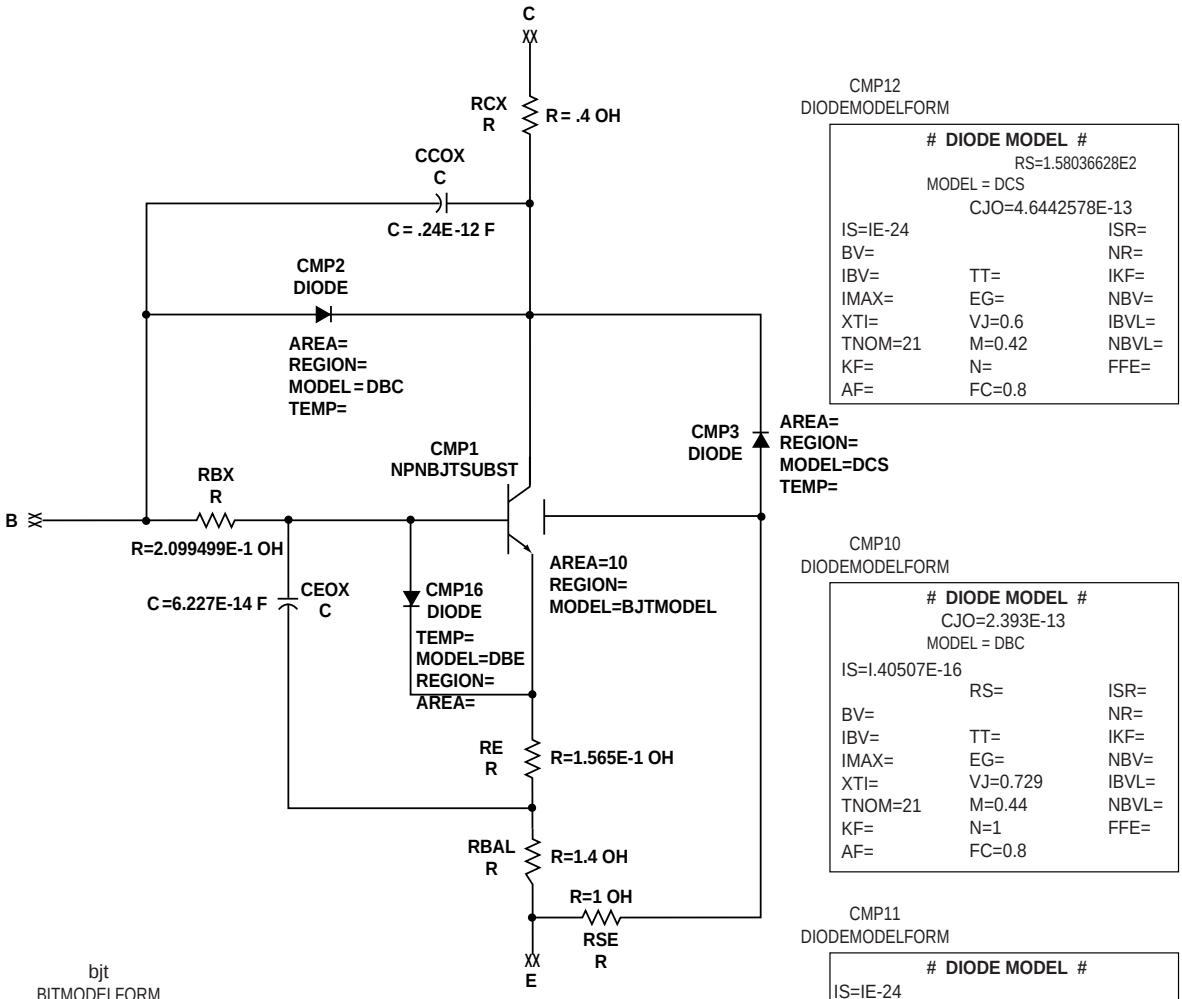
!FREQ	Fopt	GAMMA OPT		RN/Zo
!GHZ	dB	MAG	ANG	-
0.5	1.3	0.43	180	0.13
0.9	1.4	0.48	-172	0.10
1.8	1.7	0.61	-151	0.09
2.0	1.8	0.60	-149	0.11
2.5	1.9	0.61	-139	0.17
3.0	2.0	0.64	-130	0.24
4.0	2.3	0.66	-112	0.50
5.0	2.6	0.69	-93	0.88
6.0	2.9	0.73	-75	1.49
7	3.18	0.758	-56.7	2.4
8	3.51	0.789	-40.5	3.48
9	3.75	0.8	-26.3	4.3
10	4.03	0.816	-12.3	5.43

Appendix B.

Non-Linear Model



SOT343 Package Equivalent Circuit



CMP12
DIODEMODELFORM

# DIODE MODEL #		
	RS=1.58036628E2	
MODEL = DCS		
	CJO=4.6442578E-13	
IS=IE-24		ISR=
BV=		NR=
IBV=	TT=	IKF=
IMAX=	EG=	NBV=
XTI=	VJ=0.6	IBVL=
TNOM=21	M=0.42	NBVL=
KF=	N=	FFE=
AF=	FC=0.8	

CMP10
DIODEMODELFORM

# DIODE MODEL #		
	CJO=2.393E-13	
MODEL = DBC		
IS=I.40507E-16		
	RS=	ISR=
BV=		NR=
IBV=	TT=	IKF=
IMAX=	EG=	NBV=
XTI=	VJ=0.729	IBVL=
TNOM=21	M=0.44	NBVL=
KF=	N=1	FFE=
AF=	FC=0.8	

CMP11
DIODEMODELFORM

# DIODE MODEL #		
IS=IE-24		
MODEL = DBE		
	CJO=2.59257503E-13	
	RS=	ISR=
BV=		NR=
IBV=	TT=	IKF=
IMAX=	EG=	NBV=
XTI=	VJ=0.8971	IBVL=
TNOM=21	M=2.292E-1	NBVL=
KF=	N=1.0029	FFE=
AF=	FC=0.8	

bjt
BITMODELFORM

# BJT MODEL #					
MODEL = BJTMODEL				CJC=1.87E-14	
NPN=yes				ISE=5E-19	
PNP=				IS=3.01E-17	
				CJE=9.48E-14	
Forward	Reverse	Diode and junction		Parasitics	Noise
BF=1E6	BR=1	EG=1.17		RB=9.30144818E-1	
IKF=1.4737E-1	IKR=1.1E-1		VJC=.6775	IRB=3.029562E-5	AF=
	ISC=	IMAX=	MJC=0.3319	RBM=.01	KB=
NE=1.006	NC=2	XTI=3	XCJC=4.39790997E-1	RE=	AB=
VAF=4.4E1	VAR=30.37	TNOM=21	FC=0.8	RC=	FB=
NF=1	NR=1.005				KF=
TF=5.3706E-12	TR=4E-9				
XTF=20		Substrate	VJE=0.9907		
VTF=0.8		ISS=	MJE=0.5063		
ITF=2.21805486E0		NS=	CJS=		
PTF=22			VJS=		
XTB=0.7			MJS=		
APPROXOB=yes					

HBFP-0450 Die Model and SPICE Parameters

This model can be used as a design tool. It has been tested on MDS for various specifications. However, for more precise and accurate design, please refer to the measured data in the HBFP-0450 data sheet. For future improvements, Hewlett-Packard reserves the right to change these models without prior notice.

www.hp.com/go/rf
For technical assistance or the location of your nearest Hewlett-Packard sales office, distributor or representative call:

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Far East/Australasia: Call your local HP sales office.

Japan: (81 3) 3335-8152

Europe: Call your local HP sales office.

Data Subject to Change

5968-2788E (2/99)