HEWLETT® PACKARD

High-Frequency Transistor Primer

Part III-A

Thermal Resistance

A Guide to Understanding, Measuring, and Applying Power FET Thermal Resistance Coefficients

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NOTE:
Not all Hewlett-Packard part numbers mentioned herein may be available. Contact your HP representative for current product offerings.

I. Introduction

The operating temperature of a microwave power FET is an important factor affecting both RF performance and service lifetime (MTTF). Accurate determination of device channel temperatures under working conditions is essential to the power amplifier designer. With a knowledge of ambient temperature, DC bias conditions, and RF power levels, channel temperature may be calculated using the thermal resistance (θ_c) factor.

A common error is to assume that θ_{jc} is a constant. In fact, thermal resistance varies as a function of device temperature, DC bias levels, and device geometry. Processing and assembly variations are also a factor. Channel temperature calculations which assume an invariant thermal resistance may give values far from the actual operating temperature.

Thermal resistance is one of the most important parameters given in a transistor data sheet, but it is often specified ambiguously, resulting in a value which is of little or no practical use to the device user. The majority of manufacturers' data sheets give values for θ_{jc} without specifying either the measurement techinque used or related test conditions. Thermal resistance values may vary by a factor of two or more depending on these associated parameters.

If the unwary designer uses a value of thermal resistance without knowing under what conditions it was measured, both the performance and the reliability of the final design may suffer.

This paper attempts to clarify the test techniques and definitions used by Hewlett-Packard to specify the thermal resistance of its microwave power devices. Useful information is provided to allow our customers to accurately calculate both the thermal resistance and channel temperature of our devices under the operating conditions they will experience during actual use.

II. A Brief Look At Thermal Resistance and Its Measurement

A. What is Thermal Resistance?

The thermal resistance factor may be used to compute the channel temperature of a FET under a given set of operating conditions, i.e., case (flange) temperature, DC bias, and RF power level.
Thermal resistance, illustrated in Figure II-1, is defined as:

$$\theta_{jc} = \frac{T_{ch} - T_c}{P_d} \qquad \text{(Eq. II-1)}$$

where:

- θ_{jc} = channel to case thermal resistance (°C per watt)
- T_{ch} = channel temperature (highest or average) (°C)
- T_c = case or flange temperature (°C)
- P_d = power dissipated by the device, which is equal to the DC input power plus RF input power - RF output power (watts)
  - = $V_{DS} \times I_{DS} + P_{IN} - P_{OUT}$

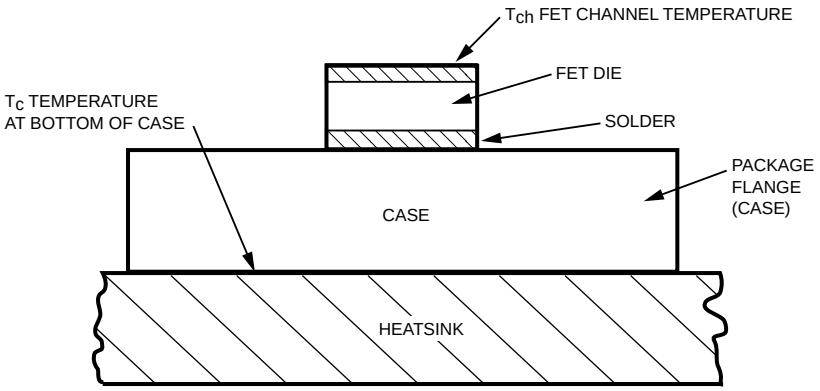


Figure II-1. Power FET Channel-To-Case Thermal Resistance

For power devices the surface of the case (flange) in contact with the heatsink is assumed to be at a constant temperature. The channel temperature, on the other hand, may vary from point to point along the active surface. This is a very important consideration as it implies that one may have more than one value of thermal resistance for the same device, measured under the same conditions, depending on the definition of channel temperature used.

At HP, we specify the so-called “hot-spot” values of thermal resistance. These values are measured using the channel temperature measured at its hottest point (a spot several μm in diameter). The advantages of using this definition will be discussed later.

B. Why is Thermal Resistance an Important Parameter?

As mentioned before, thermal resistance may be used to compute device channel temperatures when given DC, RF, and case temperature conditions. The service lifetime of the device is a strong function of channel temperature. Manufacturers typically supply plots of mean-time-to-failure vs. channel temperature for their devices.

RF performance is also affected by operating temperature. When operating FETs at elevated case temperatures, degradations in gain, efficiency, and power output must be considered.

C. How is Thermal Resistance Measured?

Several methods are used to measure thermal resistance values in both R&D laboratory and production environments. In the laboratory the number of devices evaluated is small and measurement accuracy is of prime importance. Infrared microscopy and the liquid crystal technique are commonly employed. On the production floor large numbers of sealed devices must be tested using a quick, non-destructive measurement technique. The delta V_{gs} method satisfies both these requirements.

Infrared microscopy[II-1,2,3] is one of the most widely used techniques for determining thermal resistance. A specialized microscope fitted

with infrared optics is used to detect IR emissions from the device under test (DUT). The IR radiation passes through focusing lenses onto a detector which produces an electrical output proportional to the magnitude of the IR input.

This technique is capable of ±0.5 degree Celsius accuracy and has an imaging spot size of about 15 microns in diameter. A disadvantage of this method is that the DUT must be coated with a constant emissivity coating such as lampblack. Computer driven systems are becoming available which alleviate the need for coating the sample. [II-4]

The liquid crystal technique uses a thin coating of temperature sensitive nematic crystals on the surface of the DUT to measure temperatures. A specially equipped optical microscope is used to determine channel temperatures by observing changes in the polarization of light reflected from the DUT.

Temperature accuracy is ± 0.5 degrees Celsius, and hot spots smaller than two microns can be resolved. This excellent resolution is useful in detecting small hot spots.

The delta V_{gs} method [II-5], unlike the other two precedures mentioned above, does not require coating the DUT with any sort of material. Thermal resistances are determined using the (almost linear) temperature dependent voltage drop across the gate-source diode while in forward conduction. The rapid speed, ability to test sealed devices, and non-destructive nature of this test make it ideal for production line testing. The delta V_{gs} technique is not intended for use in making absolute measurements of θ_{jc}. Rather, it is used as an indicator of die to case attach quality.

D. Interpreting the Data

It is important to realize that each of the aforementioned test techniques will yield different values of thermal resistance for the same device. An obvious precursor to interpreting data from thermal resistance testing is understanding the nature of the measurement techniques. To this end, the following sections of this application note present detailed information on both the liquid crystal and delta V_{gs} techniques.

A common misconception is that thermal resistance is a constant. This is not so! Both theory and measurements show it to be a function of device bias conditions and temperature. This application note presents both theoretical calculations and measurement data which may be used to apply the data from thermal resistance testing to determine temperatures which the device will encounter under typical operating conditions.

E. Problems with Manufacturers' Thermal Resistance Specifications

A look at power FET data sheets from several manufacturers will show that thermal resistance numbers are given without any mention of either the measurement technique used or related test conditions.

Thermal resistance measurements performed using the delta V_{gs} method may yield values several times lower than those determined using the liquid crystal technique. Device bias and temperature conditions also affect thermal resistance. Without the aforementioned information, it is difficult to compare the thermal performance of devices from different manufacturers.

At Hewlett-Packard, we specify the so-called "hot-spot" thermal resistance, measured using the liquid crystal technique. This is the most useful measure of thermal resistance as it permits the amplifier designer to determine the maximum channel temperature with a minimum of effort. The high temperature accuracy and good spatial resolution of this measurement technique coupled with the ability to perform measurements under actual device operating conditions assure realistic values of thermal resistance.

III. The Liquid Crystal Measurement Technique

A. Introduction

The liquid crystal technique finds use in laboratory applications where very fine spatial resolution and good absolute temperature accuracy are required. The spatial resolution afforded by this technique exceeds that of the more commonly used infrared method by more than an order of magnitude. Temperature may be measured to within ±0.5 degrees Celsius. The exceedingly fine spatial resolution makes possible the detection of very small (2 μm diameter) hot spots.

B. How It Works

The liquid crystal method makes use of the properties of several types of temperature sensitive bi-refringent nematic crystals. As shown in Figure III-1, the nematic-intrinsic (N-I) transition temperature, the molecules which make up the material form an orderly (nematic) array. When the transition temperature is reached or exceeded the molecules take on random (isotropic) orientations. This N-I temperature is dependent on the molecular structure of each type of nematic crystal.

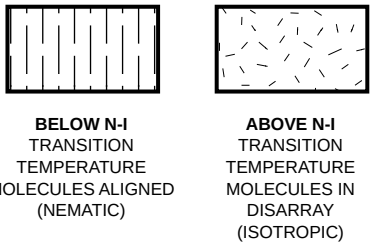


Figure III-1. The Temperature Dependent State of Liquid Crystal Molecules

This effect is utilized as follows: assume that light with a uniform linear polarization is directed towards a sample whose surface has been coated with a thin layer of nematic crystals. Let us view the reflected light from the sample through a polarizing plate which we will call the analyzer as shown at the top of Figure III-2.

If the sample is below the transition temperature, the molecules will be in an orderly (nematic) array. In this state the material is bi-refringent. Reflected light from the surface of the material will contain components polarized in two directions. Since the analyzer cannot simultaneously cancel both components, it will have little effect on the intensity of the reflected light and the sample will appear relatively bright.

Next, assume part of the sample is heated to or above the transition temperature. The crystal molecules will move into a random (isotropic) arrangement. Reflected light will have a uniform linear polarization. If

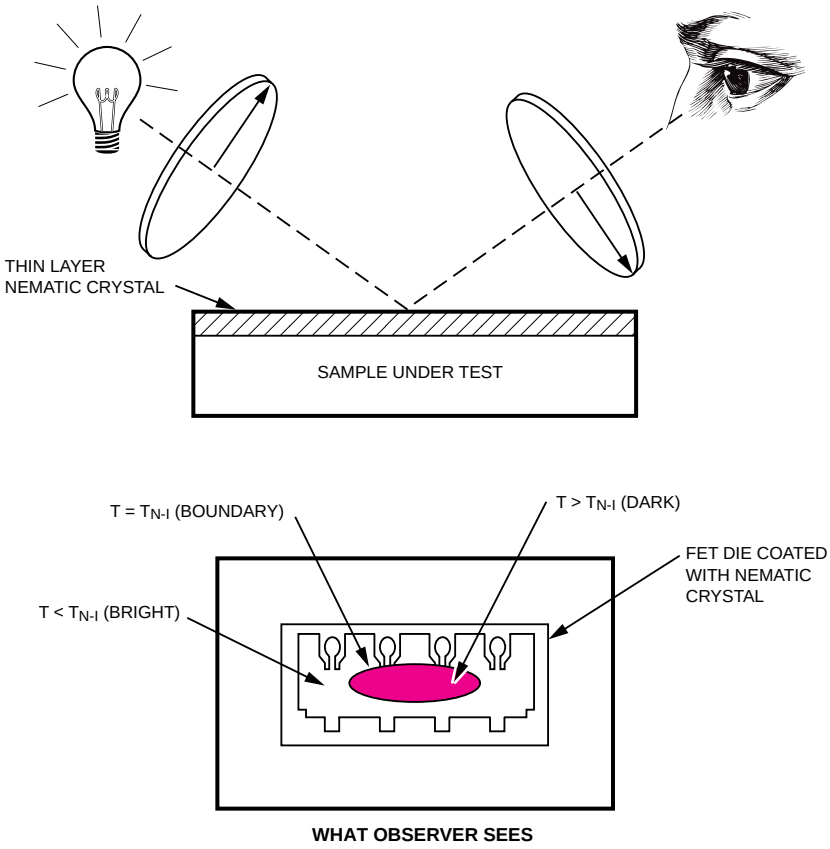


Figure III-2. Simplified Liquid Crystal Viewing

the analyzer is oriented correctly, almost all of the reflected light will be attenuated. Thus, that part of the DUT which is at or above the N-I transition temperature will appear dark, as shown at the bottom of Figure III-2.

C. How To Use It

A diagram of a typical setup used to perform liquid crystal testing is shown in Figure III-3. An optical microscope is equipped with two polarizing plates; a fixed orientation polarizer is located just after the light source and a rotatable analyzer is located in the path of the light reflected from the device under test (DUT).

A hot/cold plate is placed on top of the microscope stage to bring the DUT to the desired testing temperature. DC power supplies are used to apply bias to the device. A camera may be used to record heating patterns of the DUT. Figure III-4 shows a photograph of the liquid crystal test setup used at Hewlett-Packard.

Nematic crystals with N-I transition temperatures ranging from 50 to 240 degrees Celsius may be obtained from several manufacturers*. The material is typically supplied in powdered form.

Figure III-5 shows the steps necessary to prepare and apply a liquid crystal solution to the DUT. First, a small quantity of nematic crystal

*
E. Merck Laboratories
500 Executive Blvd.
Elmsford, NY 10523

Eastman Kodak Co.
Rochester, NY 14650
1-800-225-5572
(Technical Information)
1-800-225-5352 (Orders)

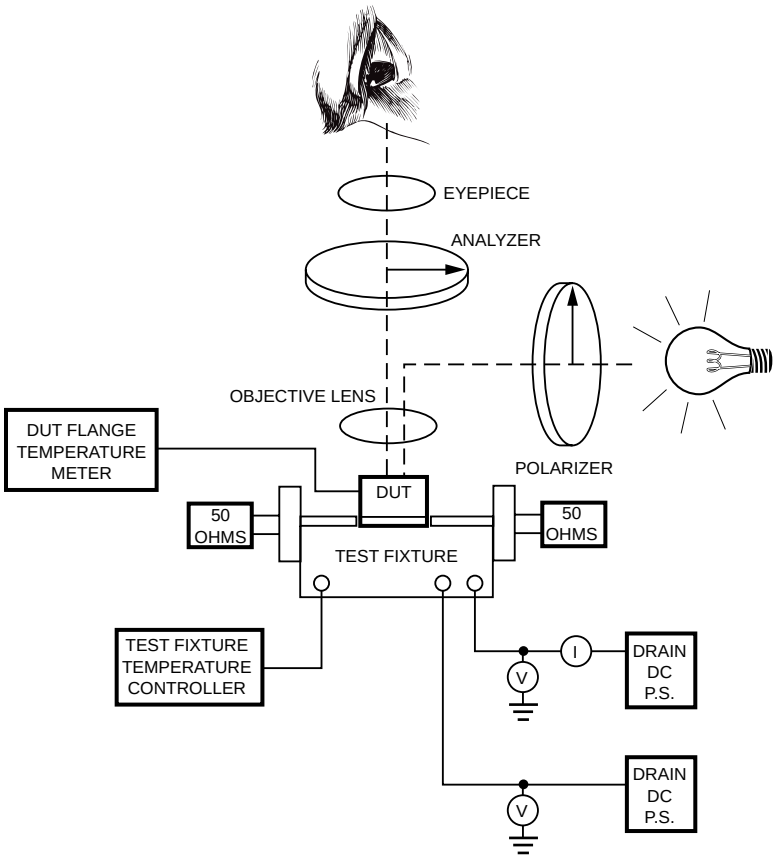


Figure III-3. Block Diagram of a Liquid Crystal Test Setup

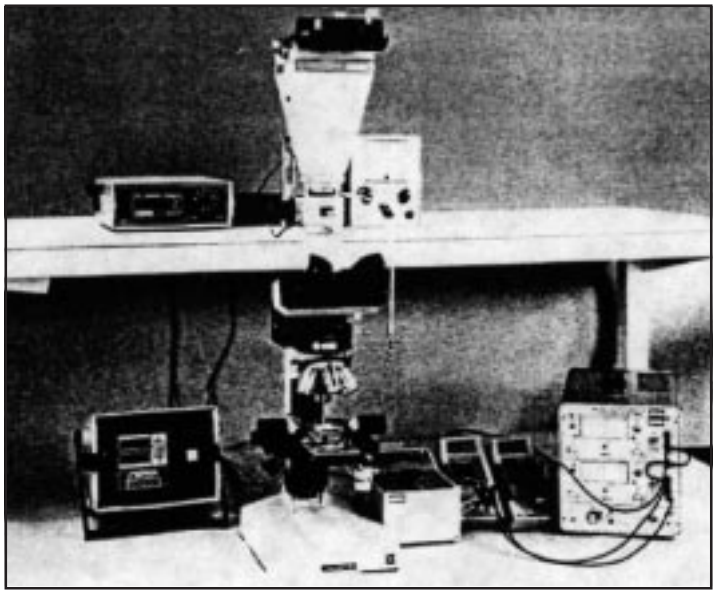


Figure III-4. Liquid Crystal Test Setup used at Hewlett-Packard

powder is added to a carrier liquid such as acetone. We typically use about 0.05 grams (a heaping pile on the tip of a jeweler's screwdriver) of nematic crystal powder mixed into 10 ml of acetone. Use caution since acetone is highly flammable. One must be careful not to add too much solid crystal to the carrier liquid as this will result in a thick coating caking the surface of the DUT when the solution dries. (If this happens, flood the DUT with solvent to clean it.) Next, the mixture is stirred until the powder fully dissolves. A few drops of the solution are placed onto the device to be tested. When the carrier liquid has completely evaporated the device is ready to be tested. The DUT, now ready for testing, is then placed into the hot/cold fixture and biased as desired.

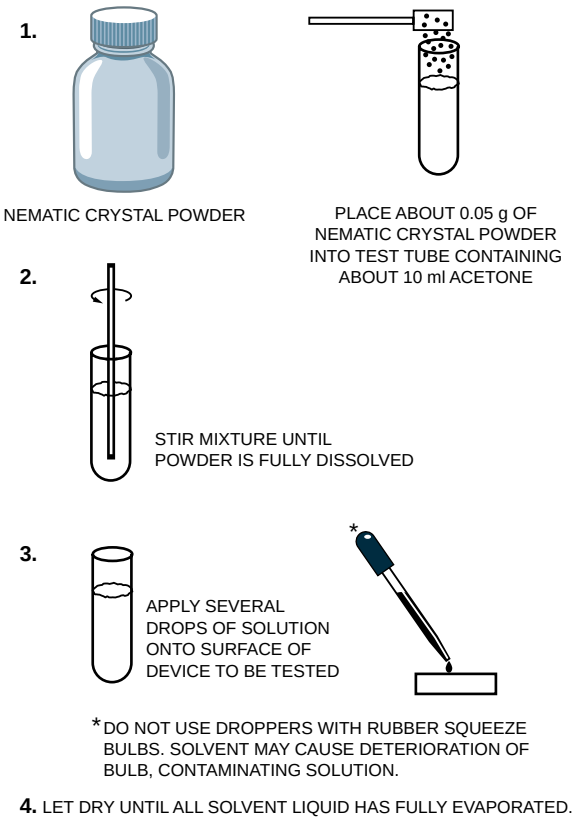


Figure III-5. Preparation and Application of Liquid Crystal Solution

The following equation is commonly used to determine the thermal resistance of the DUT:

$$\theta_{jc} = \frac{T_{ch} - T_c}{P_d} \qquad \text{(Eq. 111-1)}$$

where:

θ_{jc}	=	channel-to-case thermal resistance (°C/watt)
T_{ch}	=	channel temperature of the device under test (°C)
T_c	=	device case (flange) temperature (°C)
P_d	=	bias power plus RF input power – RF output power (watts)

If there is no RF power present, we may rewrite Eq. III-1 for the case of a FET under test as:

$$\theta_{jc} = \frac{T_{ch} - T_c}{V_{ds} I_{ds}} \qquad \text{(Eq. III-2)}$$

where:

T_{ch}	=	DUT channel temperature (°C)
T_c	=	device case or flange temperature (°C)
V_{ds}	=	drain to source voltage (Volts)
I_{ds}	=	drain to source current (Amperes)

For a backside mounted FET, the channel temperature will be virtually the same as the temperature on the surface of the die. Thus one can substitute the N-I transition temperature for T_{ch} in Eq. III-2 and solve for θ_{jc}:

$$\theta_{jc} = \frac{T_{N\text{-}I} - T_c}{V_{ds} I_{ds}} \qquad \text{(Eq. III-3)}$$

where $T_{N\text{-}I}$ is the N-I transition temperature for the crystal in use.

As the above equation indicates, the DUT can be raised to the transition temperature by changing either the ambient (case) temperature or the DC input power. Alternately increasing then decreasing the DC power provides a quick indication of how heat spreads across the surface of the device.

It should be mentioned that there has been some concern expressed as to the sensitivity of the nematic crystals to variations in electric field magnitude. As sizable field values may exist between closely spaced source, gate, and drain fingers, such concern seems warranted. In fact, the types of crystal used for temperature characterization show little or no variation as a function of electric field intensity over the range of DC values commonly applied to power FETs.

This has been confirmed via the following experiment: A FET coated with nematic crystal solution was biased to pinchoff. The drain voltage was varied at flange temperatures well below, near, and above the N-I transition temperature. The only change noticed was a slight brightening of the DUT at high drain voltages when the unit was below the transition temperature.

The source of concern may be due to confusion with a class of nematic crystals which exhibit changes at relatively low intensity electric fields. These have been used to spot pinholes and defects in semiconductor device oxide and metallization layers. [III-7, 8, 9]

D. Some Tips for Practical Measurements

Experience gained over several hundred measurements yields the following practical tips:

1. Some nematic crystals exhibit a “false” transition point below the true N-I temperature. This false point is usually far below the specified N-I temperature. The user should watch out for such points which betray themselves by resulting in calculated values of thermal resistance much greater than those expected. The higher transition temperature crystals may exhibit several such points.

2. An important factor often overlooked is the variation of thermal resistance with temperature. This should be expected since the thermal resistivity of semiconducting materials (including GaAs!) varies as a function of temperature [III-10, 11, 12]. Measurements of thermal resistance may vary over thirty percent depending on channel and substrate temperatures during testing.

   In view of this, it is desirable to use a crystal with a transition temperature close to the channel temperature which the device is expected to see in normal use. This avoids the necessity of having to calculate the thermal resistance at different channel and substrate temperatures, which may be done using Kirchoff ’s transformation [III-13] as shown in Appendix B. It is especially important to be aware of this variation with temperature when

measuring thermal resistance values for use in reliability calculations or accelerated life testing.

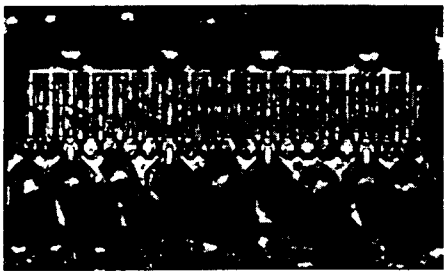
3. Thermal resistance has been observed to vary with drain-source voltage, increasing with increasing V_{ds}. Variations exceeding ten percent have been observed over a V_{ds} range spanning 2 to 11 volts [III- 14]. In view of this variation, it is desirable to measure device thermal resistances under normal operating bias conditions.

4. The DUT may be cycled above and below the transition temperature as many times as desired without degradation of crystal performance so long as the maximum temperature the sample experiences does not exceed more than about thirty degrees Celsius above the transition temperature. At elevated temperatures, the crystal sublimates and a new application of solution is required to continue testing.

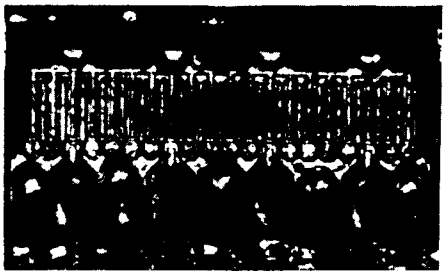
5. As the crystal is very sensitive to small changes in temperature near the N-I transition point, the user should allow sufficient time for thermal equilibrium to be established after changing either the flange temperature or DC power to the DUT. The response time of the nematic crystal is usually much faster than the thermal time constant of the DUT. Equilibrium may be observed when the boundary between light and dark areas stops moving under constant bias and flange temperature conditions. Use of a hot/cold stage with a large thermal mass (e.g., a thick copper block) will help keep DUT temperatures very stable for long periods of time.

E. Some Results

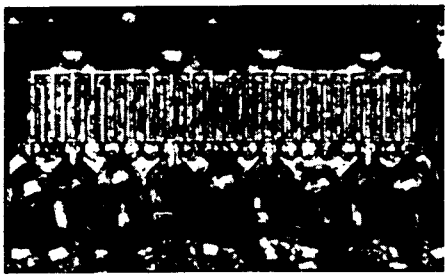
Figure III-6 shows a sequence of photographs taken of an HP AT-8141 power FET transistor chip mounted in an IMFET (98) package. (All succeeding measurements are performed using the AT-8141 unless otherwise specified.) The photos clearly show the changes in surface temperature as the device is heated. The top left photo (Figure III-6a) shows the device before heating. Photo “b” shows the appearance of the first hot spot (at or above the N-I transition temp.), on a drain finger. Succeeding photos show the expansion of the hot area as it spreads throughout the surface of the die. As expected, heating begins in the center of the die and moves outward. Note the symmetrical elliptical shape of the dark area. This is indicative of good die to flange attachment. A die which is poorly attached to its carrier may show a number of isolated hot spots, merging into one another as heating progresses.



III-6a

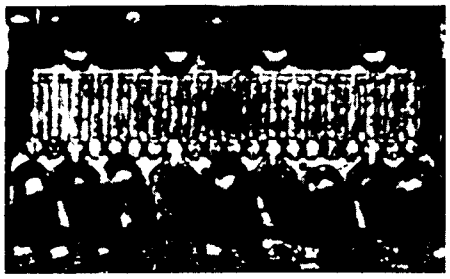


III-6d



III-6b

III-6e



III-6c

III-6f

Figure III-6.

Measurement accuracy and repeatability are enhanced by using the power and temperature conditions commensurate with the appearance of the first hot spot (Figure. III-7) when calculating thermal resistance per Eq. III-2. Since the device will most likely fail at the hottest point ***it is desirable to define thermal resistance under the conditions at which the first hot spot appears when making calculations of device reliability.***

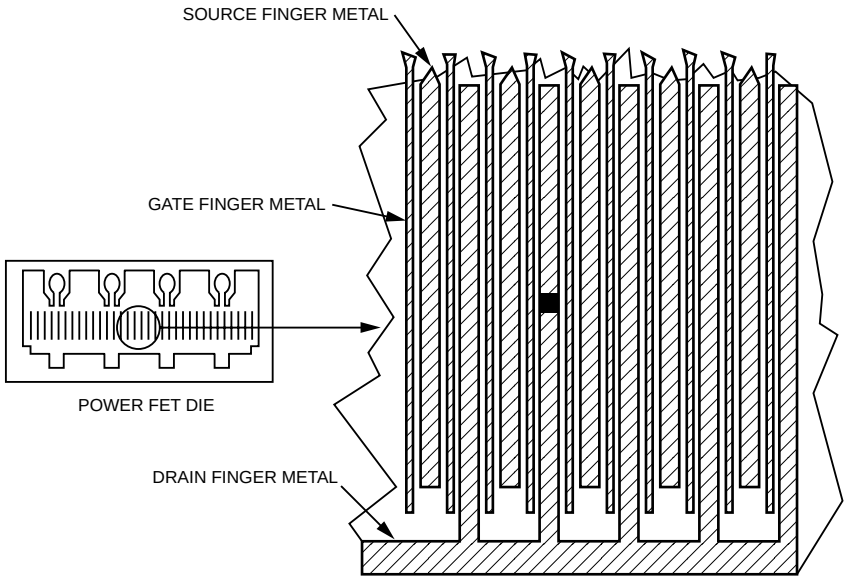


Figure III-7. Closeup of Fingers Showing Appearance of First Hot Spot

Using the liquid crystal method one may construct plots showing contours of constant temperature (isotherms) on the surface of the die under test. The isotherms are determined by using a single N-I transition temperature crystal, and varying the flange temperature in small increments. As the channel temperature increases, the dark area will increase. The boundary between the light and dark areas will be at the N-I transition temperature, and the difference between the hottest part of the die and the boundary will be given by:

$$\Delta T = T_{case1} - T_{case2} \qquad \text{(Eq. III-4)}$$

where:

T_{case1} = DUT case temperature measured when the hottest point is observed

T_{case2} = DUT case temperature

This formula assumes that the thermal resistance of the DUT is constant over temperature, a valid assumption for temperature differences on the order of several tens of degrees. Figure III-8 shows a series of isothermic contours generated from the photographs of Figure III-6.

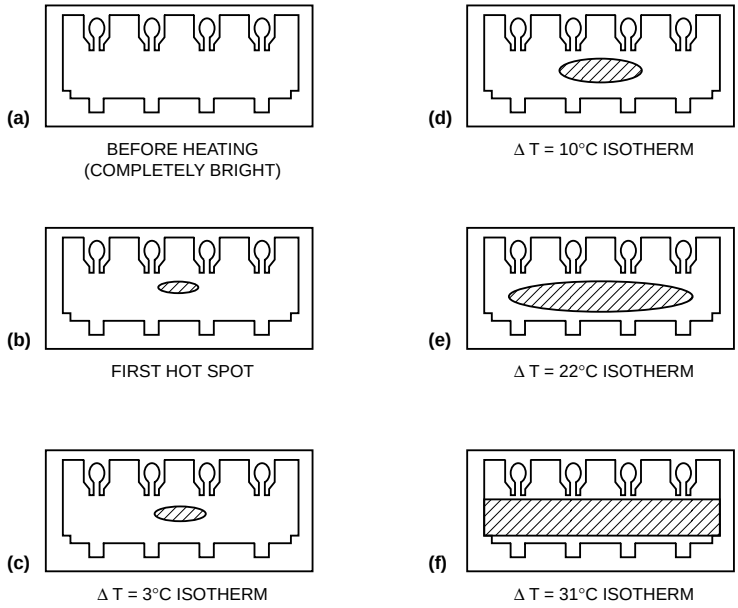


Figure III-8.

The variation of thermal resistance as a function of temperature was studied by performing hot-spot thermal resistance measurements using five different nematic crystals on the same device, each having a different N-I transition temperature. The results of these measurements are shown Figure III-9. This data was found to give excellent agreement with the values computed using Kirchoff 's transformation.

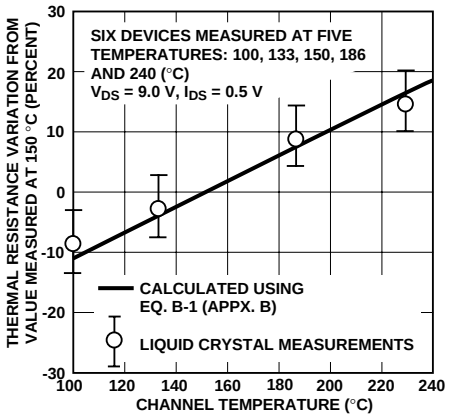


Figure III-9. Deviation of Thermal Resistance from Value at 150°C vs. Temperature

The effect of varying drain current on thermal resistance was investigated by performing hot-spot thermal resistance measurements while holding drain voltage constant. Drain current was varied by a factor of three, and case temperature was adjusted to keep the size of the hot spot constant at each value of I_{ds}. The variation of θ_{jc} due to the case temperature change was computed and subtracted from the total variation observed, yielding no net variation of thermal resistance with drain current.

An experiment was performed to determine the variation of thermal resistance as a function of drain-source voltage. V_{ds} was varied over a range spanning from 2 to 11 volts, and I_{ds} appropriately adjusted to keep the power dissipated by the DUT constant. The case temperature was set as required to keep the hot spot size constant at each set of V_{ds}, I_{ds} values. The variation of θ_{jc} due to the change in case temperature was calculated and subtracted from the thermal resistance measured, giving the variation due to changing values of V_{ds}. The results of this experiment are given in Figure III-10.

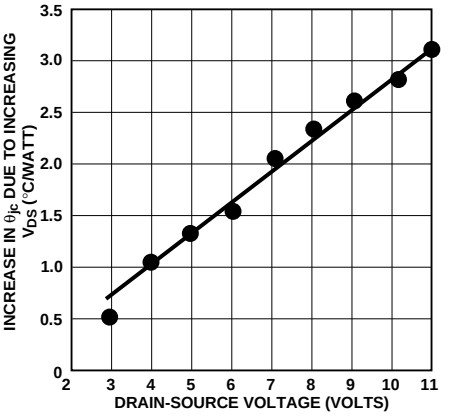


Figure III-10. Thermal Resistance vs. Drain-Source Voltage

F. Correlation With Other Methods

The excellent spatial resolution and temperature accuracy make liquid crystal measurements ideal for use as reference standards when calibrating thermal resistance measurements performed using other techniques. Liquid crystal measurements have been used at Hewlett-Packard to provide correction factors for use with delta V_{gs} measurements so that the latter may be used to give reasonable approximations of hot spot thermal resistances. Details of the correction of delta V_{gs} measurements are given in part IV.

Measurements have been performed on several devices using both the liquid crystal technique and infrared microscopy. Comparison indicates that data from the IR testing yields values of thermal resistance about ten percent lower than the values calculated using liquid crystal measurement data. This is to be expected as the IR microscope has lower spatial resolution, typically 15-30 micron spot size (spot size can be as small as 7 microns with appropriate optics), whereas the liquid crystal method can resolve hot spots on the order of several microns.

G. Summary

The liquid crystal method provides a powerful tool with which to measure the thermal resistance of microwave power devices. It offers superior spatial resolution and temperature accuracy when compared to other methods which currently find wide use. This technique permits measurements to be made which are difficult or impossible to perform using other methods. The superior spatial resolution afforded permits θ_{jc} to be defined at the onset of the first hot spot, facilitating more accurate determinations of maximum channel temperature and reliability predictions.

IV. The Delta V_{gs} Measurement Technique

A. Introduction

While not intended to give values of thermal resistance to be used in calculating operating channel temperatures, the delta V_{gs} measurement technique provides a quick, non-destructive determination of die-to-case attachment quality. This measurement, when correlated to liquid crystal measurements, may be used as a technique to guarantee the conformance of production units to thermal resistance specifications.

B. Principle of Operation

The use of the voltage drop across a forward-biased diode as an indicator of thermal performance is well documented, [IV-1, 2, 3, 4, 5, 6] and will be reviewed only briefly here for the sake of completeness.

The forward I-V characteristic of the gate-source Schottky diode may be expressed as:

$$J = AT^2 \exp\left(\frac{-qV_b}{kT}\right) \exp\left(\frac{qV}{nkT}\right) \qquad \text{(Eq. IV-1)}$$

for $V >> \frac{3kT}{q}$

where:

- J = forward current density
- A = effective Richardson constant
- T = junction temperature (K)
- q = charge of the electron
- V_b = built-in barrier voltage
- k = Boltzmann constant
- V = voltage across junction
- n = ideality factor

Eq. IV-1 may be solved for V:

$$V = nV_b - \frac{nkt}{q}\left[21nT - 1n\left(\frac{J}{A}\right)\right] \qquad \text{(Eq. IV-2)}$$

For moderate and constant values of current density J, the voltage across the junction V decreases almost linearly with increasing temperature.

We define the K factor for a device as

$$K = \frac{\Delta T}{\Delta V} \text{ (at constant current)} \qquad \text{(Eq. IV-3)}$$

which will vary depending on the specific processing involved for each type of device. K factors are measured at Hewlett-Packard by placing the DUT in an oven and measuring the voltage across the forward conducting gate-source Schottky junction at a number of different temperatures while holding I_{gs} constant at 0.1 mA. Adequate time must be given between measurements to allow the temperature to stabilize. This procedure is repeated at several different temperatures. Figure

IV-1 shows a plot of the K factor obtained for the HP M113 power FET (with a gate periphery of 10 mm).

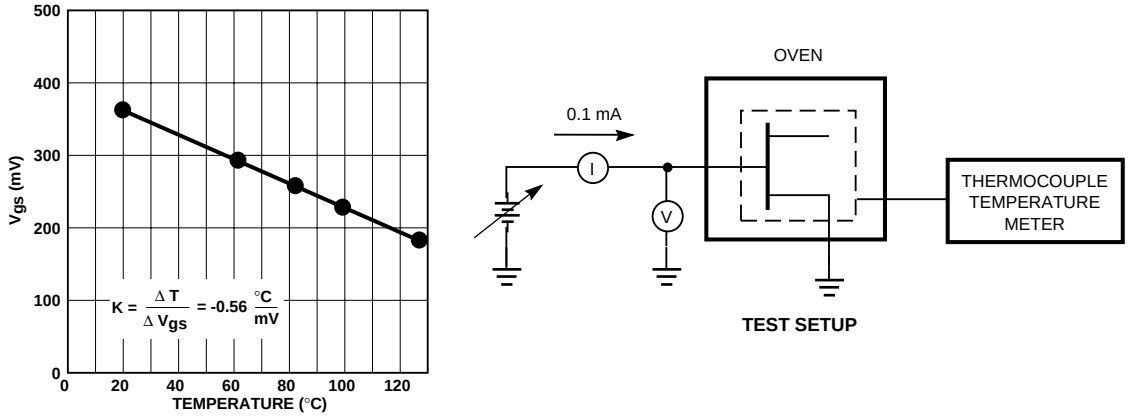
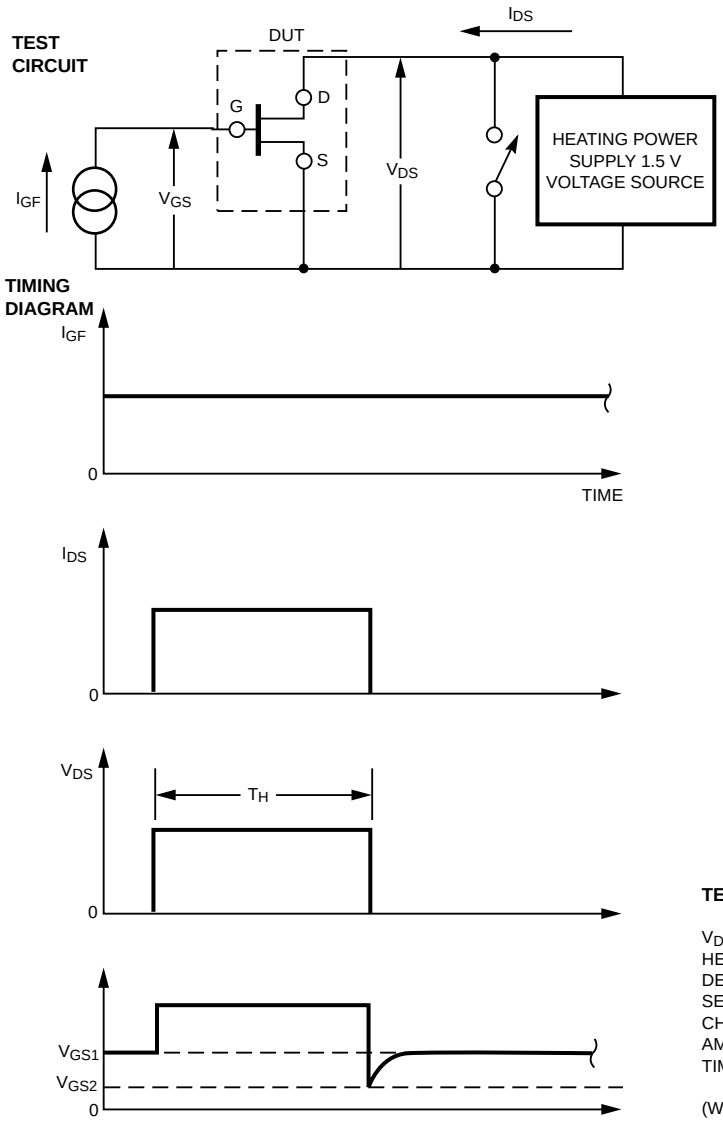


Figure IV-1. K Factor Plot for HP M113 Microwave Power FET



At HP delta V_{gs} measurements are performed using a Sage Enterprises model DAE 220. The unit provides a forward gate current through the gate-source diode and applies a voltage pulse between the drain and source to heat the device. At the end of each heating pulse, the drain and source are shorted together and a measurement of the voltage drop across the gate-source diode performed. Figure IV-2 shows a rough schematic of the setup and a timing diagram showing the relationship between the heating pulse and the measurement interval.

TEST CONDITIONS:

V_{DS} = 1.5 V, V_{GS} > 0

HEATING PULSE WIDTH (T_H):	30 msec
DELAY TIME (T_D):	2 μsec
SENSING CURRENT (I_{GF}):	0.1 mA
CHANNEL TEMPERATURE:	60°C
AMBIENT TEMPERATURE:	25°C
TIME BETWEEN HEATING PULSES (T_P):	0.5 sec

(WHEN REPETITIVE MEASUREMENTS ARE MADE)

Figure IV-2. Simplified Schematic and Timing Diagram for Delta V_{gs} Measurements

Knowing the device K factor, the amount of power supplied by the heating pulse, and the change in gate-source voltage measured from the time before the heating pulse to the time directly following it, we may compute the thermal resistance:

$$\theta_{jc} = \frac{D_{vgs} K}{V_h I_h} \qquad \text{(Eq. IV-4)}$$

where:

θjc	=	channel-to-case thermal resistance (°C/watt)
D_{vgs}	=	change in voltage across gate-source diode (from time before to time after heating pulse)
V_h	=	Drain-source heating pulse voltage
I_h	=	Drain-source heating pulse current

C. Thermal Time Constants

At this point let's step back and see what we are really measuring. The DUT consists of a number of different materials joined together, each with different thermal characteristics. An analogous electrical equivalent of this would be a circuit consisting of a number of RC circuits in series (Figure IV-3). The time constants of the RC circuits correspond to the heating and cooling "thermal time constants" of the different constituent materials of the DUT, and will be a function of the physical properties and sizes of those materials. These time constants may be both calculated and directly measured. Examples of both follow:

1. Calculation of thermal time constants

As an example, let's compute the thermal time constant of a 4 mil thick GaAs FET die. The thermal time constant is given by:

$$t = \left(\frac{2F}{\pi}\right)^2 \left(\frac{PC}{\sigma}\right) \qquad \text{(Eq. IV-5)}$$

where:

F= die thickness (cm)
p = density of the material (g/cm^3)
σ = thermal conductivity (W/cm°C)
c = specific heat of the material (J/g°C)

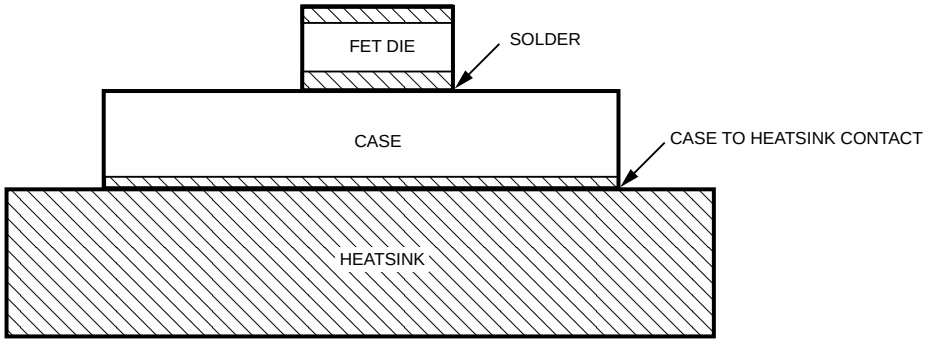
For GaAs, the appropriate values are:

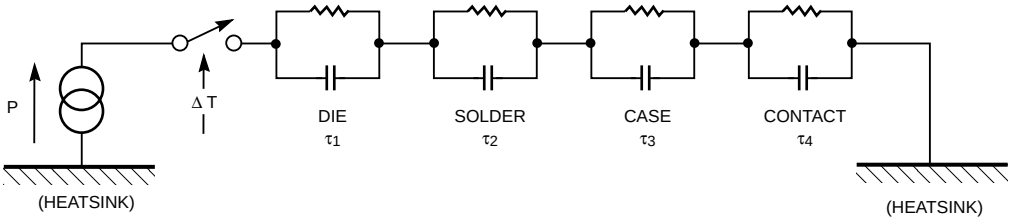
p = 5.31 g/cm^3
σ = 0.44 W/cm°C
c = 0.35 J/g°C

and F = 0.01 cm for a 4 mil thick die. Substituting the above constants into (Eq. IV-5) gives:

t = 175 µs

For a packaged device, time constants for the solder between the die and flange, and contact between the flange and test fixture or chassis may be similarly computed.





ORDER OF MAGNITUDE:

DIE THERMAL TIME CONSTANT (τ_1):	200 µsec
SOLDER THERMAL TIME CONSTANT (τ_2):	VERY SHORT FOR GOOD SOLDER
CASE THERMAL TIME CONSTANT (τ_3):	10 msec
CONTACT THERMAL TIME CONSTANT (τ_4):	0.5 sec
HEATSINK THERMAL TIME CONSTANT):	LONG, MORE THAN 5 SECONDS

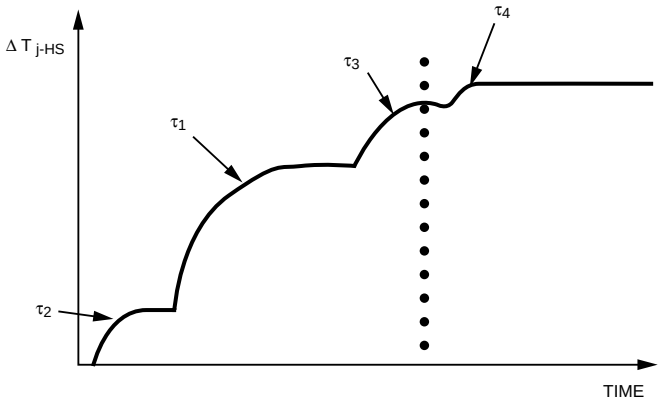


Figure IV-3. Analogous Electrical Model of Thermal Time Constants with Timing Diagram

2. Experimental Determination of Thermal Time Constants

Thermal time constants may also be evaluated experimentally. Figure IV-4 gives a plot of delta V_{gs} (linearly proportional to channel temperature) versus time for an HP 6 watt IMFET™ internally matched FET. Data was obtained by varying the heating pulse width while using a constant delay time (2 µs) between the end of the heating pulse and beginning of the V_{gs} measurement.

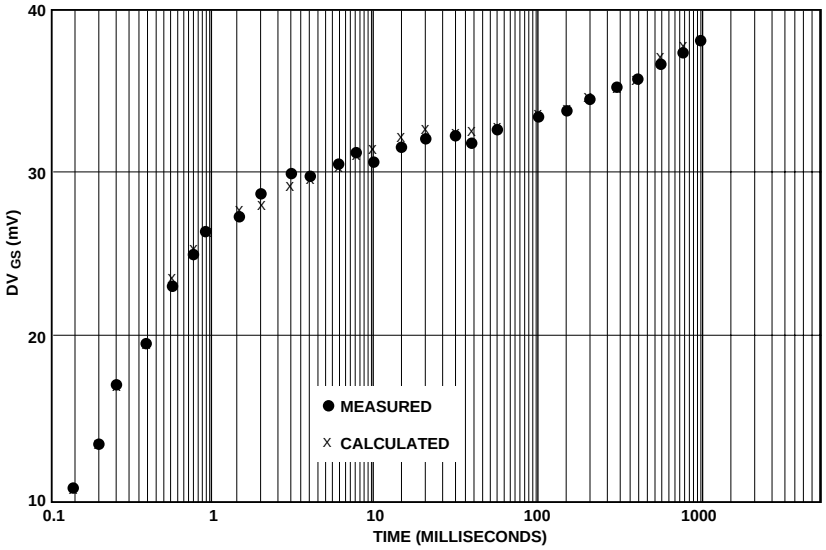


Figure IV-4. Measured and Calculated Thermal Time Constants of Internally Matched FET

We can take this experimental data and curve fit it to a form which is a sum of exponential curves. This yields the following formula giving delta V_{gs} as a function of time:

$$V_{gs} = 24.8\left[1 - \exp\left(\frac{-t}{0.262}\right)\right] + 7.3\left[1 - \exp\left(\frac{-t}{3.56}\right)\right] + 8.0\left[1 - \exp\left(\frac{-t}{658}\right)\right]$$

(Eq. IV-6)

where:

V_{gs} is in mV
t is time in msec.

Figure IV-4 shows both the measured data and delta V_{gs} as calculated using the above equation.

By comparing the time constants obtained from the experimental data to those calculated from the device material parameters we may identify the thermal time constants of the constituent members of the DUT. The first exponential in Eq. IV-6 (the smallest time constant) may be assumed to be the contribution of the FET die. The second term represents the flange, and the third the contact thermal resistance

between the flange and the heat sink (test fixture) to which the DUT is secured. The constant of the solder between the FET die and the package is probably too small to be accurately measured.

Summarizing the results for the above 6 watt IMFET device and computing thermal resistance by using Eq. IV-4 we get the following:

Component	Time Constant	Thermal Resistance
die	0.262 msec	1.85 (°C/watt)
flange	3.56	0.54
contact	658	0.60

(A good contact thermal resistance is about 0.2°C/watt. The value shown above was obtained by measuring the IMFET device in a quick-mount type fixture instead of bolting the flange down to the heatsink as would typically be done.)

Now that we have gone to all the trouble of calculating and measuring the thermal constants of our device, one may ask “What do we do with this data?” Aside from giving us some physical insight as mentioned above, knowledge of the thermal time constants will help us to perform more accurate measurements by allowing us to: (1) choose proper heating pulse widths, and (2) correct for the cooling which occurs between the end of the heating pulse and the beginning of the delta V_{gs} measurement.

The length of the heating pulse must be carefully chosen so that only the desired components of the DUT are heated. One does not want to inadvertently include the case-to-heatsink (device case-to-test fixture) contact thermal resistance in a measurement of channel-to-case thermal resistance. The dotted line in the plot at the bottom of Figure IV-3 shows the point at which the heating pulse should be terminated and delta V_{gs} measurement initiated so as not to include the contact thermal resistance in the measurement.

The DUT will begin to cool during the time between the end of the heating pulse and beginning of the delta V_{gs} measurement. A short delay is required between these two steps to allow circuit switching transients to die out. The resulting measurement error (about 10% for an IMFET device) may be corrected by measuring the thermal time constant of the DUT and extrapolating back to the time at which the heating pulse just ends.

Knowledge of the thermal time constants also allows us to know just which components within the device are heating and lets us judge the effects of changing flange, solder, and device parameters when optimizing thermal performance.

D. Corrections to the Raw Data

Having looked at the principle behind delta V_{gs} measurement and given some advice on how to perform it, we come to the point at which we have the results of the tests in our hands and must interpret the data. This is the most important part of the whole process! There are several important points regarding the delta V_{gs} method which must not be overlooked to fully understand the results of the measurement. SEVERAL CORRECTIONS TO THE VALUE OF θ_{jc} GIVEN IN EQ. IV-4 ARE REQUIRED TO OBTAIN THE TRUE VALUE OF THERMAL RESISTANCE THAT A DEVICE WILL EXPERIENCE AT THE OPERATING POINT IT WILL SEE IN NORMAL USE:

It is important for the user of delta V_{gs} measurements to be aware of the following:

1. ***The delta V_{gs} method gives a value of thermal resistance corresponding to a temperature which is averaged over an unknown fraction of the active area of the FET. Thermal resistance calculated using uncorrected delta V_{gs} measurement data is not representative of the temperature at the hottest point on the die.*** Uncorrected delta V_{gs} measurements provide a relative measurement which is useful in assessing the quality of the die attachment to the package. The delta V_{gs} technique is used primarily to determine the die attach quality of large numbers of devices in a production environment, not to determine absolute values of thermal resistance. It is possible to correlate this averaged value to the peak value of thermal resistance at the hottest part of the channel using liquid crystal measurements. The liquid crystal technique, described in part III of this application note, has spatial resolution exceeding 2 microns, and may be used to measure the thermal resistance at the hottest part of the DUT. Both liquid crystal and delta V_{gs} measurements are performed on a number of devices. A correlation factor is thus obtained relating the peak to average thermal resistance values.

2. Thermal resistance varies as a function of drain-source voltage. The Sage DAE 220 places 1.5 volts across the drain and source to heat the DUT. Typical operating drain-source voltages for power FETs may range from 8 to 10 volts. A heating pulse voltage at this level would subject the DUT to excessive electrical stress (drain current would exceed I_{dss} as the gate is forward biased). The higher value of V_{ds} might also result in high amplitude oscillations which may destroy the device.

   Liquid crystal measurements may be performed at several drain voltages to obtain correction factors for each type of device to translate the value of θ_{jc} obtained with the delta V_{gs} method to actual operating voltages. A plot of θ_{jc} vs. V_{ds} is given in Figure III-10 of section III.

3. Thermal resistance measured using the delta V_{gs} method is usually performed at a single value of flange and channel temperature. To translate this to other temperatures, correction is required. The variation of thermal resistance of semiconducting materials with

temperature is well known.[IV-7, 8, 9, 10] One may use Kirchoff's transformation [IV-11] to convert the value of thermal resistance at one channel temperature to another. Appendix C details the derivation of a form of Kirchoff's transformation useful for power FET calculations. Appendix B gives several useful "real-world" calculation examples.

When the following corrections:

1. Device cooling between heating and measurement
2. Peak (hot-spot) to averaged channel temperature
3. Channel temperature transformation
4. Flange temperature transformation

are all applied to the raw data produced by delta V_{gs} measurement, we arrive at the following correction formula which will give a value approximating the hot-spot value of thermal resistance:

$$\theta_{jc22} = \theta_{dvgs} \bullet K1 \bullet K2 \bullet K3 \bullet K4 \bullet K5 \bullet K6 \qquad \text{(Eq. IV-7)}$$

where

θ_{jc22} = thermal resistance at flange temperature T_{c2} and channel temperature T_2

θ_{dvgs} = thermal resistance measured by delta V_{gs} test at flange temperature T_{c1} and channel temperature T_1

K1 = factor which takes into account the cooling of the device in the time between the end of the heating pulse and the beginning of delta V_{gs} measurement during testing. For an IMFET device measured using a 2 μsec delay time, this number equals 1.1 (a 10% correction)

K2 = factor which relates the peak (hottest spot) channel temperature determined from liquid crystal measurements to the averaged channel temperature during delta V_{gs} testing. This factor is different for different device types, depending primarily on geometry.

K3 = factor which accounts for change in θ_{jc} due to change in V_{DS} from the 1.5 volt delta V_{gs} measurement to the value of V_{DS} which the device will see in actual operation. This factor also must be evaluated for each type of device. Figure III-10 is a plot of K3 vs. V_{DS} for the AT-8141.

$$K4 = \frac{T_{ch2} - T_{c2}}{T_{ch1} - T_{c1}}$$

$$K5 = \frac{\alpha 11 - T_{c1}}{\alpha 22 - T_{c2}}$$

$$K6 = \frac{a + bT_{c2}}{a + bT_{c1}}$$

where:

T_{ch2} = desired channel temperature
T_{ch1} = channel temperature during delta V_{gs} measurement
T_{c2} = desired flange temperature
T_{c1} = flange temperature during delta V_{gs} measurement
$\alpha 11$ = Kirchoff (linearized) channel temperature as defined in Eq. C-14 in Appx. C corresponding to channel temperature T_{ch1}
22 = Kirchof f (linearized) channel temperature as defined in Eq. C-15 in Appx. C corresponding to channel temperature T_{ch2}
a = thermal resistivity coefficient for GaAs doped at n = 5E16, equal to 7.043 (see Appx. C)
b = thermal resistivity slope coefficient for GaAs doped at n = 5E16, equal to 0.00828 (see Appx. C)

(All temperatures are measured in degrees Celsius)

E. Automation of the Delta V_{gs} Measurement Setup

The outstanding advantage of the delta V_{gs} method over other techniques is that measurements made using this technique are non-destructive (do not require de-lidding the DUT or coating it with any substance) and fast. This makes it ideally suited for production line thermal resistance testing. Computer control also permits the use of untrained operators to perform testing.

At present there is no commercially available automated delta V_{gs} tester suitable for microwave power FET measurement. To meet the need at Hewlett-Packard for semi-automated production line thermal resistance measurements a Sage model DAE 220 was modified to interface with a microcomputer, printer, and plotter via the IEEE-488 instrumentation bus. A block diagram of the system is shown in Figure IV-5.

The DAE 220 does not come equipped with an IEEE-488 port, but does have a centronics-type parallel I/O port which is normally used to transfer data to an external printer. An ICS Corporation model 4871 TTL to IEEE-488 conversion unit was used to interface the DAE 220 with the other IEEE-488 compatible system components. Since the DAE 220 is not equipped to generate or receive handshake signals, and the ICS 4871 might not be fast enough to handle the data from the Sage,

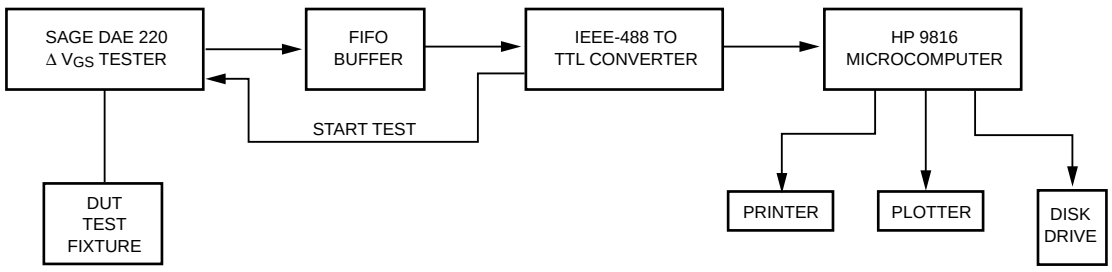


Figure IV-5. Block Diagram of Computer Controlled Delta V_{gs} Thermal Resistance Measurement Setup

a fast FIFO buffer was added between the two units. Data format conversion is handled via software. A TTL signal is sent from the computer to an open collector driver across the “TEST” switch on the Sage front panel to initiate a measurement cycle.

Test parameters such as heating voltage and pulse lengths must be manually set at the Sage front panel. Values returned from the Sage to the computer are delta V_{gs} and I_h, the heating current. For each device tested, the computer performs five identical tests then averages the data to obtain the final “raw” (uncorrected) value of thermal resistance as defined in Eq. IV-4.

Finally, the computer performs the corrections mentioned in the previous section to give a reasonable approximation of the thermal resistance for the DUT commensurate with normal operating bias and temperature levels. If a device is found to have unacceptably high thermal resistance the operator is alerted and told to reject the unit.

Figure IV-6 and Table IV-1 give examples of plotter and printer output from several typical production runs. Data may also be sent to a mass storage unit and correlated over time to monitor statistical trends.

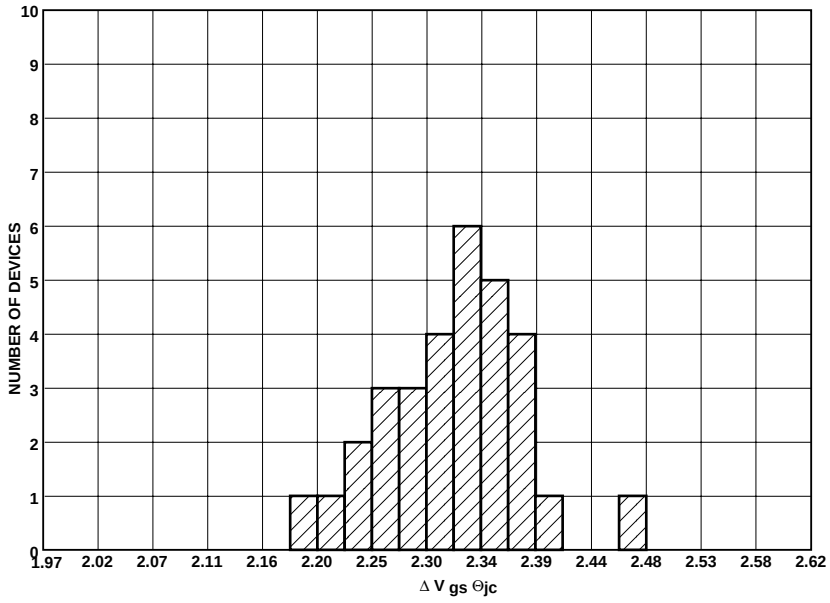


Figure IV-6. Sample of Delta V_{gs} Distribution Plot Generated Using the Setup Shown in Figure IV-5

Table IV-1. Die Attach Evaluation/Thermal Resistance Measurement

Serial Number	θ_{jc}(1.5V) (°C/Watt)	Normalized Case temp (°C/Watt)	Thermal Resistance (T_{ch} = 150°C, T_{case} = 70°C V_{DS} = 9 V)
1	2.34	2.26	5.77
2	2.43	2.36	6.00
3	2.46	2.37	6.04
4	2.36	2.28	5.80
5	2.41	2.34	5.93
6	2.47	2.38	6.07
7	2.32	2.24	5.71
8	2.40	2.32	5.91
9	2.34	2.27	5.77
10	2.46	2.37	6.03
11	2.45	2.36	6.00
12	2.57	2.48	6.32
13	2.43	2.33	5.94
14	2.49	2.40	6.12
15	2.27	2.19	5.57
16	2.40	2.31	5.89
17	2.41	2.36	5.94
18	2.40	2.31	5.89
19	2.14	2.31	5.89
20	2.30	2.21	5.62

F. Summary

An overview of the delta V_{gs} method of thermal resistance measurement has been presented including theory of operation along with methods of interpreting and correcting the raw data. Details of an automated delta V_{gs} test station suitable for production use have been given.

It should be stressed that delta V_{gs} measurements are best used as a means of determining die attach quality. The method is not intended to give absolute values of thermal resistance commensurate with the typical operating conditions of the DUT. For this purpose, liquid crystal measurements should be used. Using the correction techniques discussed above it is possible to correlate delta V_{gs} and liquid crystal measurements to some degree, but again it should be stressed that the delta V_{gs} method is not intended to give absolute values of θ_{jc}.

Appendix A.
Thermal Resistance Data for HP IMFET Internally Matched FETs

Table A-1

HP IMFET™ Internally Matched GaAs FET Family (Watts)	Typical R_{jc} at Recommended Bias Point @ t channel = 150°C [1] (°C/W)
1.5	19.9
3	11.5
6	5.3
8	6.5
2[2]	8.8
4[2]	5.1

Notes: 1. Measured using 150° N-I Liquid Crystal, at hottest spot.
2. High Frequency

Appendix B.
Using Thermal Resistance Data: Some Practical Examples

Thermal resistance is not a constant. Determining the correct value at actual device operating channel and case temperatures requires several corrections to the thermal resistance values given in device data sheets. This appendix gives several examples showing how to correct thermal resistance values to account for temperature variations. Note that the following corrections do not take into account any changes in thermal resistance due to variations in drain-source voltage. The examples given below assume operation at the values of V_{ds} listed in the thermal resistance specifications of Hewlett-Packard product data sheets. Operation at other values of V_{ds} may require additional correction as indicated in section III of this application note.

Kirchoff's transformation may be applied to determine the value of thermal resistance at one channel temperature when given the value at another. The thermal resistance of GaAs may be approximated as a linear function of temperature over the range of power FET operation. Applying the appropriate terms from Appendix C, Eq. C-13, the thermal resistance at channel temperature T_{ch2} and case (flange)

temperature T_{c2} may be determined from value given in the catalog, measured at T_{ch1} and T_{c1}, by using the following relation:

$$\theta_{jc2} = (\theta_{jc1} - \theta_{case})\left(\frac{246.7 + T_{ch2}}{246.7 + T_{ch1}}\right)\left(\frac{T_{ch2} - T_{c2}}{T_{ch1} - T_{c1}}\right)\left(\frac{\alpha 11 - T_{c1}}{\alpha 22 - T_{c2}}\right) + \theta_{case} \quad \text{(Eq. B-1)}$$

where:

θ_{jc2} = Channel to case thermal resistance at channel temperature T_{ch2} and case temperature T_{c2}

θ_{jc1} = Channel to case thermal resistance at channel temperature T_{ch1} and case temperature T_{c1}

θ_{case} = Thermal resistance of case, from bottom of flange to the top surface which the FET die rests upon. θ_{case} for several HP IMFET products is given in Table B-1.

$$\alpha 11 - T_{c1} + (246.7 + T_{c1}) \ln\left(\frac{246.7 + T_{ch1}}{246.7 + T_{c1}}\right) \quad \text{(Eq. B-2)}$$

$$\alpha 22 - T_{c2} + (246.7 + T_{c2}) \ln\left(\frac{246.7 + T_{ch2}}{246.7 + T_{c2}}\right) \quad \text{(Eq. B-3)}$$

This formula is also given in Hewlett-Packard IMFET product data sheets.

Table B-1.

Device Type (Watts)	θ_{case} (°C/Watt)
1.5	2.0
2	1.1
3	1.1
4	0.7
6	0.7
8	0.6

Note that θ_{jc1} and θ_{jc2} represent the total (FET plus case) thermal resistance of the device. The thermal resistance of the case is subtracted from the total thermal resistance before performing the temperature correction, then added in after correction. This is because we wish to correct only the GaAs FET thermal resistance. The case thermal resistance remains essentially constant with temperature. (Here we are assuming a perfect contact between the FET die and the case.)

If we desire to determine the ***channel-to-heatsink*** thermal resistance, the case to heatsink contact thermal resistance must be added to θ_{jc}. This contact thermal resistance is equal to approximately 0.22°C/watt for HP IMFET internally matched FETs.

Eq. B-1 may be used with a programmable calculator or PC to give a quick estimation of the thermal resistance of a device under actual operating conditions. The following examples demonstrate the most common applications involving temperature corrected thermal resistance:

For convenience, Hewlett-Packard power product data sheets include plots of channel vs. case temperature as shown in Figure B-1. These plots are constructed using the above formulation of Kirchoff's transformation. Using these plots avoids the necessity of performing the calculations shown in examples 1 and 2 below.

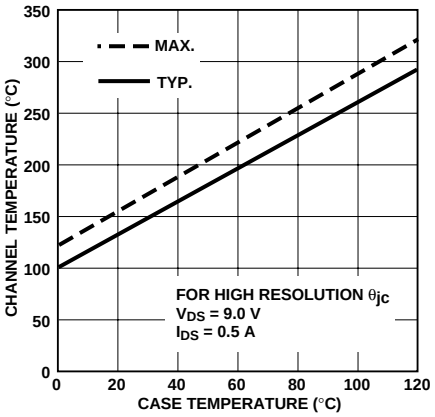


Figure B-1. Plot of Case vs. Channel Temperature

Several examples are now given illustrating how to use Eq. B-1 to find the case and channel temperatures and thermal resistance, under several real-world conditions.

Example 1: Determination of maximum heatsink temperature
Suppose we wish to operate an HP IM-6471-1.5 IMFET internally matched power FET at a channel temperature of 200°C, biased at 9 V, 0.5 A. What will the maximum permissible heatsink temperature be? Using Eq. B-1 along with the equation defining thermal resistance:

$$\theta_{jc} = \frac{T_{ch} - T_c}{V_{ds} I_{ds}} \qquad \text{(Eq. B-4)}$$

where:

θ_{jc} = channel to case thermal resistance at channel temperature T_{ch} and case temperature T_c.

The values of θ_{jc} and related measurement conditions listed in the Hewlett-Packard data sheet for this device are:

θ_{jc} (max.) = 23.0°C/watt

measured with:

channel temperature (T_{ch})	= 150°C
case temperature (T_c)	= 46.5°C
drain-source voltage	= 9.0 V
drain-source current	= 0.5 A

To determine the temperature of the heatsink, we must add the thermal resistance of the contact between the flange and the heatsink to the channel-to-case thermal resistance. Measurements indicate that typical case-to-heatsink thermal resistance for an IMFET power FET package is 0.22°C/watt. Thus, the last term in Eq. B-1 becomes θ_{case} + 0.22.

We may write a small program to solve Equations B-1 and B-4 iteratively, or write a program to solve Eq. B-1, then plug the resulting

values of θ_{jc} into Eq. B-4, continuing manually until a satisfactory solution is reached. This is illustrated as follows:

First, assign values to the variables in Eq. B-1:

T_{ch1} = 150 (From the product data sheet)
T_{c1} = 46.5
θ_{jc1} = 23.0

and:

θ_{case} = 2.0 (from Table 1 above)
T_{ch2} = 200 (the desired channel temp.)

For a first guess, try the value of T_{c2} = 70°C. Inserting this and the catalog values above into Eq. B-1 yields θ_{jc2} = 25.41°C per watt.

Now insert this value for θ_{jc} along with V_{ds} = 9.0 and I_{ds} =0.5 (the measurement conditions given in the data sheet) into Eq. B-4 and solve for the channel temperature:

$T_{ch} = T_c (\theta_{jc} \bullet V_{ds} \bullet I_{ds})$

$= 70 + (25.41) \bullet (9.0) \bullet (0.5)$
$= 184.3°C$

This is too low. To get closer to the desired value of T_{ch} = 200°C let's try a flange temperature of 80°C. Solving Eq. B-1 gives θ_{jc} = 25.75°C per watt. Substituting this into Eq. B-4 gives T_{ch} =195.87°C. This is much closer. Continuing the process for several more iterations gives the final value of case temperature:

$T_{heatsink_{max}}$ = 83.6°C

Example 2: Determination of maximum channel temperature
Equations B-1 and B-4 may be used to determine the channel temperature for a given heatsink temperature. Let us compute the maximum channel temperature commensurate with a heat-sink temperature of 60°C for an IM-6471-1.5 IMFET device.

As in the previous example, we take the values of θ_{jc1}, T_{ch1}, and T_{c1} from the catalog. We substitute these along with the desired flange temperature T_{c2} into Eq. B-4 and solve for the thermal resistance θ_{jc2}.

From the IM-6471-1.5 data sheet:

θ_{jc1} = 23.0
T_{ch1} = 150
T_{c1} = 46.5

and:

θ_{case} = 2.0 (from Table 1 above)
T_{c2} = 60.0 (the desired case temp.)

As in the previous example, let us take the case-to-heatsink thermal resistance to be equal to 0.22°C/watt. Let us try T_{ch2} = 175 as a first guess at the channel temperature. Solving Eq. B-1 gives θ_{jc2} = 24.37°C/watt. Substituting this value into Eq. B-4 gives:

$$T_{ch} = T_c + (\theta_{jc} \bullet V_{ds} \bullet I_{ds})$$
$$= 60 + (24.37) \bullet (9.0) \bullet (0.5)$$
$$= 169.68°C$$

This is below the 175 we guessed, so next time, let's try inserting T_{ch2} = 168 into Eq. B-1. This yields θ_{jc2} = 24.18°C/watt, which in turn yields T_{ch} = 168.8°C. This is very close to the value of channel temperature we put into Eq. B-1. Further iterations yield the final value of channel temperature:

$$T_{ch} = 168.9°C$$

Comparison of Calculated and Measured Variation of θ_{jc} with Temperature

Figure B-2 gives a plot comparing the calculated change in thermal resistance versus channel temperature with measured values. The change in thermal resistance is given as a percentage, relative to the value measured at 150°C. The empirical curve shows data taken from measurements of a single AT-8141 transistor chip mounted in an IMFET (98) package using a succession of five different liquid crystal solutions, each with a different N-I transition temperature. The calculated curve was obtained by substituting the measured value of thermal resistance at 150°C for θ_{jc1} in Eq. B-1 and computing θ_{jc2} at the other temperatures shown. Comparison shows very good agreement between the measured and calculated values.

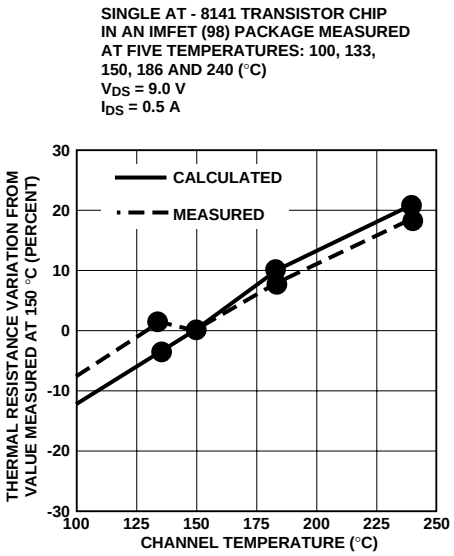


Figure B-2. Calculated and Measured Thermal Resistance vs. Channel Temperature

Appendix C.
Kirchoff's Transformation

The variation of semiconductor thermal conductivity with temperature is well known. [C-1, 2, 3, 4] The thermal resistance of power FETs is usually specified at a single value of flange and channel temperature, which may not be representative of conditions which the device will encounter during normal use. Given the thermal resistance at one flange and channel temperature, Kirchoff's transformation[C-5] may be used to determine the thermal resistance at other temperatures. In this appendix, a form of the transformation useful in performing power FET thermal calculations is derived.

We define the thermal resistance between two points as:

$$\theta_{12} = \frac{\Delta T_{12}}{P_d} \qquad \text{(Eq. C-1)}$$

where:

θ_{12} = Thermal resistance between points 1 and 2
ΔT_{12} = Temperature difference between points 1 and 2 (T_2-T_1)
P_d = Power dissipated by heat source (heat flux through isothermic surfaces 1 and 2)

The thermal conductivity of many materials, including semiconductors, varies as a function of temperature, i.e.,

$$\sigma = \sigma(T) \qquad \text{(Eq. C-2)}$$

To find the thermal resistance for these materials, one must solve the general non-linear heat flow equation

$$\nabla \cdot \sigma \nabla T = 0 \qquad \text{(Eq. C-3)}$$

at the two points of interest in order to find ΔT to substitute into Eq. C-1. By using Kirchoff's transformation we may define a "linearized" temperature throughout the material such that at each point x we associate a value

$$\alpha(x) = T_o + \frac{1}{\sigma_o}\int_{T_o}^{T} \alpha(T)\, dT \qquad \text{(Eq. C-4)}$$

with the true temperature T(x)

where:

$\alpha(x)$ = the linearized temperature at point x
σ_o = thermal conductivity at $T = T_o$

For power FETs $\alpha(x)$ may be thought of as the value the channel temperature would equal if the thermal conductivity of GaAs were a constant ($\sigma = \sigma_o$) over temperature.

The thermal resistivity of gallium arsenide has been measured over the temperature range spanning 300 to 1000 Kelvin for several levels of doping concentration by Amith et. al.[C-1]. Using this data we may express the thermal conductivity of GaAs as:

$$\alpha\,(T) = \frac{1}{a + bT} \qquad \text{(Eq. C-5)}$$

Values of the constants a and b are given in Table C-1 for several values of doping concentration.

Table C-1. a and b Constants for GaAs (Amith et. al.[C-1])

N (cm^{-3})	a (°C cm/W)	b (cm/W)
5E16	2.043	0.008280
4E17	2.106	0.009154
8E18	2.289	0.011177

Substituting Eq. C-5 into Eq. C-4 and solving for the linearized channel temperature corresponding to channel temperature T_{ch1} and case (flange) temperature T_{c1}:

$$\alpha 11 = \alpha\,(T_{ch1} + T_{c1}) = T_{ch1} + \frac{1}{\sigma\,(T_{c1})} \int_{T_{c1}}^{T_{ch1}} \sigma\,(T)\,dT$$

$$= T_{c1} + (a + bT_{c1}) \int_{T_{c1}}^{T_{ch1}} \frac{dT}{a + bT}$$

$$= T_{c1} + (a + bT_{c1})\ \frac{1}{b}\left[\ln\,(a + bT)\right]_{T_{c1}}^{T_{ch1}}$$

$$\alpha 11 = T_{c1} + \left(\frac{a}{b} + T_{c1}\right) \ln\left(\frac{a/b + T_{ch1}}{a/b + T_{c1}}\right) \qquad \text{(Eq. C-6)}$$

Using the definition of thermal resistance given in Eq. C-1 to solve for the linearized channel temperature we get:

$$\alpha 11 = T_{c1} + P_d \bullet \theta(\alpha 11) \qquad \text{(Eq. C-7)}$$

where $\theta(\alpha 11)$ is the linearized thermal resistance corresponding to the linearized channel temperature $\alpha 11$. This is the value which the thermal

resistance would have if the thermal conductivity of the material did not vary with temperature. We may express $\theta(\alpha 11)$ as:

$$\theta(\alpha 11) = R_{th}(T_{ch1}) \bullet G \qquad \text{(Eq. C-8)}$$

where $R_{th}(T_{ch1})$ is equal to the thermal resistivity of the material at a temperature of T_{ch1} ($R_{th}\{T_{ch1}\} = a + bT_{ch1}$), and G is a factor dependent on device geometry.

We want to find the channel-to-case thermal resistance, defined as:

$$\theta_{jc} = \frac{T_{ch} - T_c}{P_d} \qquad \text{(Eq. C-9)}$$

Substituting Eq. C-7 into Eq. C-9 and solving for θ_{jc}:

$$\theta_{jc11} = (\theta_{jc}(T_{ch1}, T_{c1}) = \frac{T_{ch1} - T_{c1}}{P_d} = \frac{\Delta T_{11} \bullet \theta(\alpha_{11})}{\alpha_{11} - T_{c1}} \qquad \text{(Eq. C-10)}$$

where:

θ_{jc} = FET channel-to-case thermal resistance for $T_{ch} = T_{ch1}$ and $T_c = T_c$

ΔT_{11} = $T_{ch1} - T_{c1}$

Similarly, for $T_{ch} = T_{ch2}$ and $T_c = T_{c2}$ we may write

$$\theta_{jc22} = \frac{\Delta T_{22} \bullet \theta(\alpha_{22})}{\alpha 22 - T_{c2}} \qquad \text{(Eq. C- 11)}$$

A multiplicative factor relating thermal resistance at $R_{ch} = T_{ch1}$ and $T_c = T_{c1}$ to the value at $T_{ch} = T_{ch2}$ and $T_c = T_{c2}$ is found by taking the ratio:

$$R_{21} = \frac{\theta_{jc22}}{\theta_{jc11}} = \frac{\left(\frac{\Delta T_{22} \bullet \theta(\alpha 22)}{\alpha 22 - T_{c2}}\right)}{\left(\frac{\Delta T_{11} \bullet \theta(\alpha_{11})}{\alpha 11 - T_{c1}}\right)}$$

$$R_{21} = \left(\frac{\Delta T_{22}}{\Delta T_{11}}\right)\left(\frac{\theta(\alpha 22)}{\theta(\alpha 11)}\right)\left(\frac{\alpha 11 - T_{c1}}{\alpha 22 - T_{c2}}\right) \qquad \text{(Eq. C-12)}$$

Substituting Eq. C-5 and Eq. C-8 into Eq. C- 12 gives:

$$R_{21} = \left(\frac{T_{ch2} - T_{c2}}{T_{ch1} - T_{c1}}\right)\left(\frac{a + bT_{c2}}{a + bT_{c1}}\right)\left(\frac{\alpha 11 - T_{c1}}{\alpha 22 - T_{c2}}\right) \qquad \text{(Eq. C-13)}$$

As the active layer is very thin in comparison with the semi-insulating portion of the die, the values of a and b in Table C-1 for n = 5E16 are commonly used. Substituting these values into Eq. C-6 gives the linearized channel temperature, α 11, corresponding to $T_{ch} = T_{ch1}$ and $T_c = T_{c1}$:

$$\alpha 11 = T_{c1} + (246.7 + T_{c1}) \ln\left(\frac{246.7 + T_{ch1}}{246.7 + T_{c1}}\right) \qquad \text{(Eq. C-14)}$$

Similarly, at $T_{ch} = T_{ch2}$ and $T_c = T_{c2}$:

$$\alpha 22 = T_{c2} + (246.7 + T_{c2}) \ln\left(\frac{246.7 + T_{ch2}}{246.7 + T_{c2}}\right) \qquad \text{(Eq. C-15)}$$

We may substitute the above values of α from Eq. C-14 and Eq. C-15 into Eq. C-13 to determine the thermal resistance at a new channel temperature, which is much more representative of the actual temperature which the DUT will see in normal operation. Examples demonstrating the use of Kirchoff's transformation in real-world situations commonly encountered by the power amplifier designer are given in Appendix B of this application note.

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