HEWLETT® PACKARD

High Frequency Transistor Primer

Part III

Thermal Properties

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Preface

This is the third part of the Hewlett-Packard High Frequency Transistor Primer series. It is intended as an introduction to the thermal characteristics of GaAs FET and silicon bipolar transistors for the microwave engineer. The contents are based on the questions most often asked of members of the HP transistor group.

Using the information in this primer should enable the engineer to make the basic calculations necessary to assure that the transistors he uses will be operated at a safe temperature for long term reliability. Further discussion on the subject of transistor thermal characteristics and heat flow calculations is provided in the literature referenced in the appendix.

The other parts of the High Frequency Transistor Primer currently available are:
Part I, *Silicon Bipolar Electrical Characteristics*;
Part II, *Noise and S-Parameter Characterization*;
Part IIIA, *Thermal Resistance* and
Part IV, *GaAs FET Characteristics.*

I. Thermal Resistance

A. Definition

A transistor, bipolar or FET, has a maximum temperature which cannot be exceeded without destroying the device or at least shortening its life. The heat is generated in a bipolar transistor directly under the emitters and very close to the upper surface of the die. In the microwave FET heat is also dissipated near the surface, under the gate and near the drain end. For all practical purposes, the heat can be considered as generated on the top surface of the chip or die.

The ability of a transistor to dissipate heat depends upon a factor called the thermal resistance, which may be designed as θ, or θ_{th} or R_{th}. It is defined as follows:

Temp. Rise $\triangleq$ Power Dissipated x Thermal Resistance

$$\Delta T = P_D \theta \qquad (1a)$$

$$\theta \triangleq \frac{\Delta T}{P_D} \qquad (1b)$$

Note that θ has the dimensions of °C/watt. The reciprocal of thermal resistance is thermal conductance. Equation 1a can be used to

calculate the temperature rise at the surface of a chip due to P_D watts being dissipated, with the bottom of the chip held at a constant temperature. Junction temperature, T_j, is given as:

$$T_j = T_A + \text{Temp. rise due to heating}$$
$$T_j = T_A + P_D\theta \quad (2a)$$

where T_A is ambient temperature.

Figure 1 shows a cross section of a chip on a mount. As can be seen, there are actually three thermal resistances involved, and

$$T_j = T_A + P_D\left(\theta_{chip} + \theta_{solder} + \theta_{mount}\right) \quad (2b)$$

Note that the thermal resistances add just like electrical resistances in series. We will now see how thermal resistance is calculated.

B. Calculation of Thermal Resistance

All materials will conduct heat to some degree, some much better than others. Silver is the best metallic heat conductor and plastics tend to be relatively poor heat conductors. BeO (beryllia) is the best ceramic heat conductor and is often used in high power transistor packages.

When thermal resistance is calculated, the physical size and placement of the chip and mount are all important. There are two general cases for thermal resistance [1].

Case I - "Columnar" Heat Flow (Figure 2)*
Figure 2 shows that if the thickness of the material is small compared to the lateral dimensions of the device and die, the heat will flow in a vertical "column." The thermal resistance is then:

$$\theta_{col} = \frac{F}{K_{TH}\,\text{Area}} = \frac{F}{K_{TH}\,4CD} \quad (3a)$$

Example:
A silicon transistor 20 x 20 mils is fabricated on a die 50 mils square and 5 mils thick. Then 2D = 2C = 20 mils, 2B = 2A = 50 mils, and F = 5 mils.

$$\frac{F}{B} = \frac{5}{25} = 0.2; \frac{F}{D} = \frac{5}{10} = 0.50 \quad (3b)$$

Heat flow is, therefore, essentially columnar. See Equation 3c.

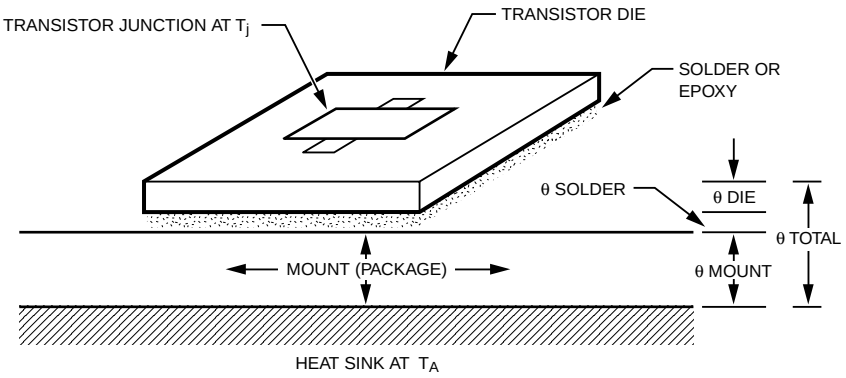


Figure 1. Transistor Thermal Resistances

Table 1. Thermal Conductivity (K_{TH}) of some Materials used in Transistors

Material	K_{TH} W/cm°C
Silicon	1.00 – 1.46
GaAs (Gallium Arsenide)	0.44
Copper	4.05
Gold	3.09
Kovar	0.2
Sapphire	0.25
Al_2O_3 (Aluminum Oxide)	0.188
BeO (Beryllium Oxide)	2.34
Silver	4.14

Equation 3c:

$$20\,\text{mils} = 0.051\,\text{cm}$$
$$\text{Let } K_{TH} = 1.0\,\text{W/cm°C}$$
$$5\,\text{mils} = 0.0127\,\text{cm}$$
$$\theta = \frac{0.0127}{1.0\left(0.051\right)^2} = 4.88\,°\text{C/W}$$

*The notation using a 2X multiplier for the dimensions is consistent with the figures in the reference.

Case II - “Spreading” Heat Flow (Figure 3)
If the material is thick compared to the device size, and the device dimensions are less than 20% of the die side dimension, then flow is said to be essentially spreading.

Figure 3 illustrates this case and shows how the heat “spreads out” instead of flowing in a vertical column. For this case:

$$\theta_{sp} = \frac{1}{K_{TH}\pi r}, r = \frac{C+D}{2} \qquad (4)$$

Note that r is the radius of a circle whose diameter is the average of the transistor dimensions.

Most transistor dimensions fall into a range of values which are intermediate between spreading and columnar flow, and the general equations for heat flow in 3 dimensions, X, Y, and Z, must be solved using the three-dimensional Laplace equation:

$$\frac{\partial^2 T}{\partial X^2} + \frac{M^2 T}{\partial Y^2} + \frac{M^2 T}{\partial Z^2} = 0 \qquad (5a)$$

Linstead and Surty [2] solved Eq. 5a for a number of different geometries and presented the results in a series of normalized charts (Figures 4, 5, 6). The use of these charts can be demonstrated as follows. The dimensional notation corresponds to Figure 3.

The dimensions of a representative transistor are 1.1 x 3.0 mils; the die is 10 mils square and about 5 mils thick. Therefore, in Figure 5:

$$2A = 2B = 0.01" = 0.0254\ cm$$
$$2D = 0.003" = 0.00762\ cm$$
$$2C = 0.0011" = 0.0028\ cm$$
$$F = 0.005" = 0.0127\ cm$$
$$\frac{A}{F} = 1,\ \frac{A}{B} = 1,\ \frac{C}{A} = 0.11,\ \frac{D}{C} \cong 3 \qquad (5b)$$

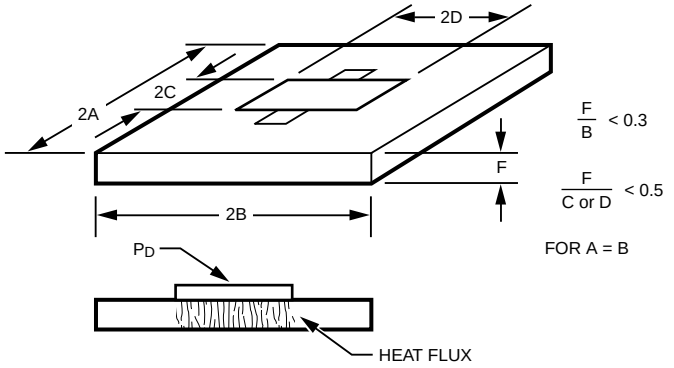


Figure 2. Columnar Heat Flow

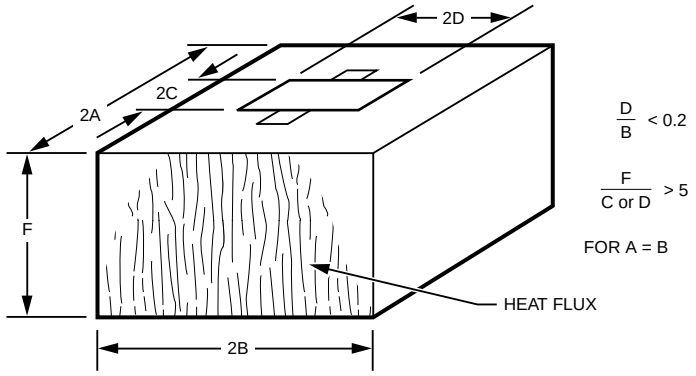


Figure 3. Spreading Heat Flow

In Figure 5, at C/A 0.11 and on the A/F = 1 curve read

$$\frac{\theta K_{TH} CD}{F} = 0.046 \qquad (5c)$$

Therefore resulting in Equation 5d, shown below.

Equation 5d :

$$\theta = \frac{0.046F}{K_{TH}CD} = \frac{0.046\left(0.0127\right)}{1.00\left(0.0014\right)\left(0.0038\right)} = 109°C/W$$

The thermal resistance for an FET cannot be calculated from the charts of Linstead and Surty since the heat source is a long thin line, not a small rectangle. Thermal resistance for a long thin line can be approximated by the analogy between fringing capacitance for an electrical conductor and thermal heat flow spreading. Since the capacitance per unit length of a transmission line is $(120\ \pi\varepsilon)/Zo$, formulas for transmission line characteristic impedance may be used to calculate thermal resistance. Using the formula for stripline characteristic impedance given by Cohn [3] and the equivalent ideal line as shown by Oliver [4], one can derive the following equation for FET thermal resistance:

$$\theta W_g = \frac{K(k)}{2 K_{TH}(K(k'))} \quad (6)$$

*

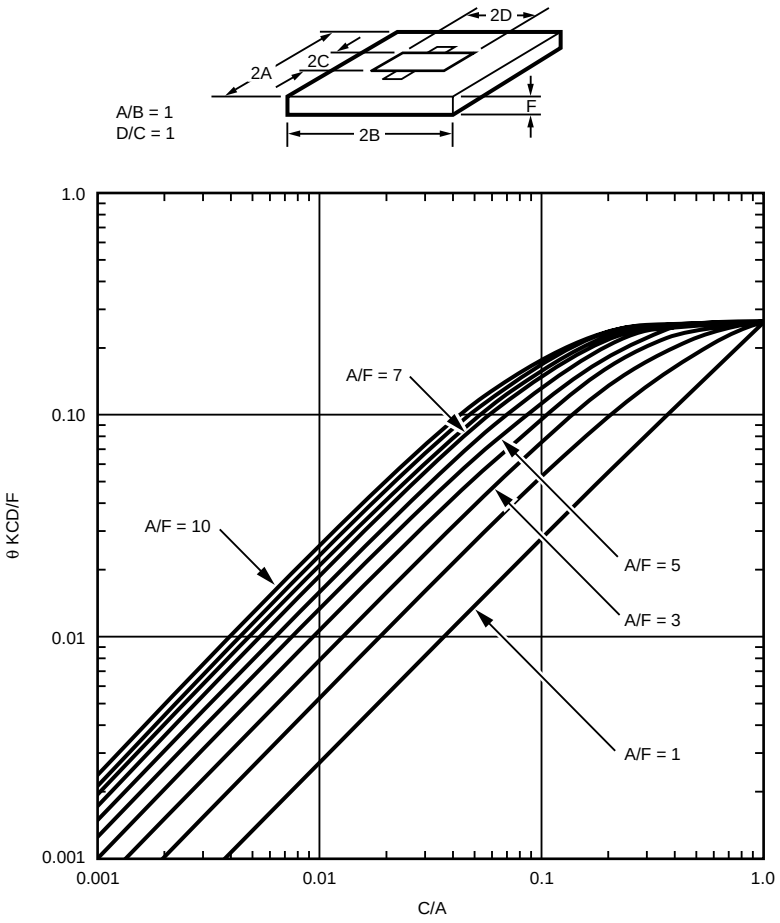


Figure 4. Thermal Resistance Curves

Where:

$$k = \operatorname{sech}\left[\frac{\pi L_g}{4F}\right] \quad (7)$$

$$k' = \tanh\left[\frac{\pi L_g}{4F}\right] \quad (8)$$

K = complete elliptic integral of 1st kind
L_g = gate length in cm
F = die thickness in cm ≅ 0.0125 cm
W_g = gate width in cm
K_{TH} ≅ 0.44, for GaAs

Using these numbers, θW_g has been calculated for gate lengths of 0.1 to 4 µm and is shown in Figure 7. Thermal resistance for three FETs has been calculated and is shown in Table 2.

Thermal resistance curves for semiconductor chips from R.D. Linstead and R.J. Surty, "IEEE Transactions on Electron Devices," Volume - ED- 19, No. 1, January 1972, pp. 41-44, Reproduced courtesy of the Institute of Electrical and Electronics Engineers. (Figures 4, 5, 6)

* Equation 6 is valid for single line gates. Devices with multiple gates (such as power FETs) could have a higher thermal resistance. This is because the gates are thermally "coupled," i.e., there is heat - transfer between gate segments.

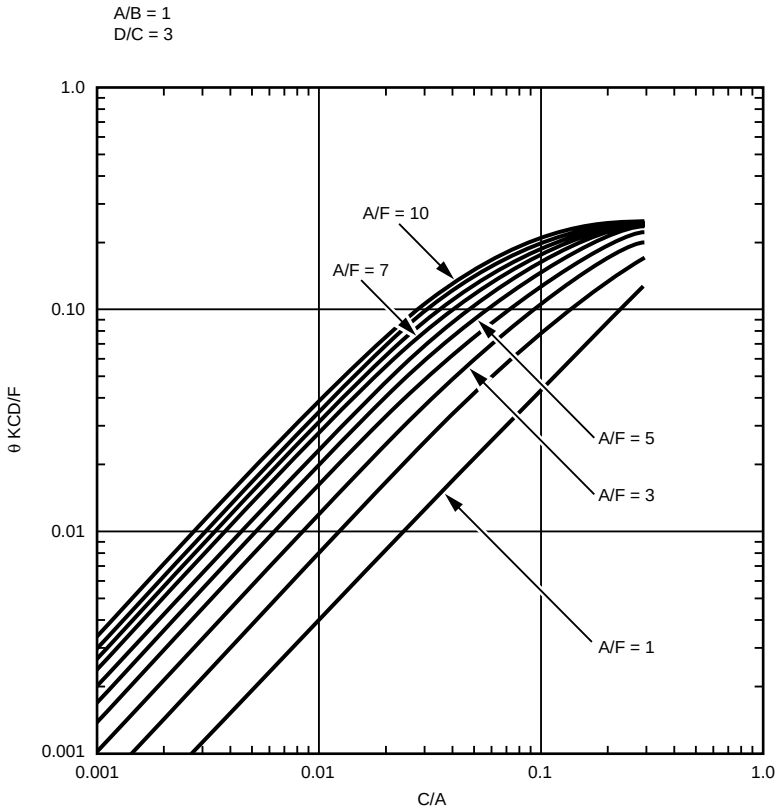


Figure 5. Thermal Resistance Curves

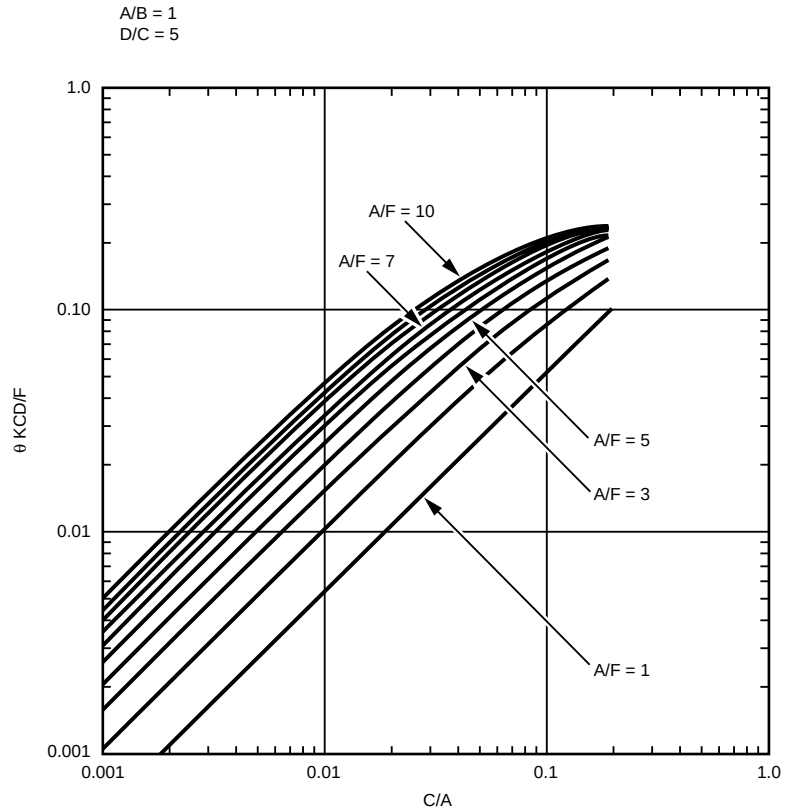


Figure 6. Thermal Resistance Curves

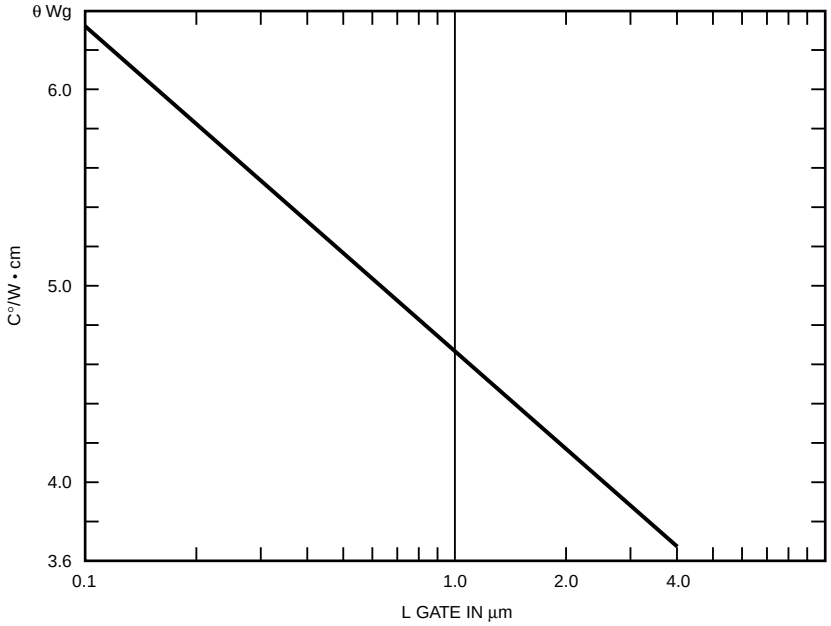


Figure 7. Thermal Resistance x Gate Width vs. Gate Length for GaAs FETs on 5 mil Thick Die

Table 2. Thermal Resistance Calculated for Two Different FETs

Device	L_g (μm)	W_g (μm)	θWg From Fig. 7 (°C cm/ W)	θ (°C/ W)
ATF-13	0.5	250	5.17	206
ATF-10	0.5	500	4.68	93.6

II. Thermal Time Constant

If a pulse of power is supplied to a semiconductor device, the temperature of the junction does not rise instantaneously. In other words, the die has a thermal time constant. Figure 8a illustrates the effect; 8b shows the electrical analog of several time constants in cascade (i.e., in series).

Semiconductor junction temperature as a function of time can be given as shown in Equation 9: *

Equation 9:

$$T_j = P_D\theta\left[\frac{4}{\pi^{\frac{3}{2}}}\right]\left[\frac{t}{\tau}\right]^{1/2} + T_A \text{ for } t < \tau$$

τ = thermal time constant

τ = time

Note that the temperature is proportional to the square root of time and, thus, the RC analog is not exact. It has also been found that Eq. 9 is only accurate during the early part of the pulse, and is not correct for the entire duration, particularly near the end as the temperature approaches equilibrium, i.e., as t approaches τ.

The thermal time constant can be estimated by:

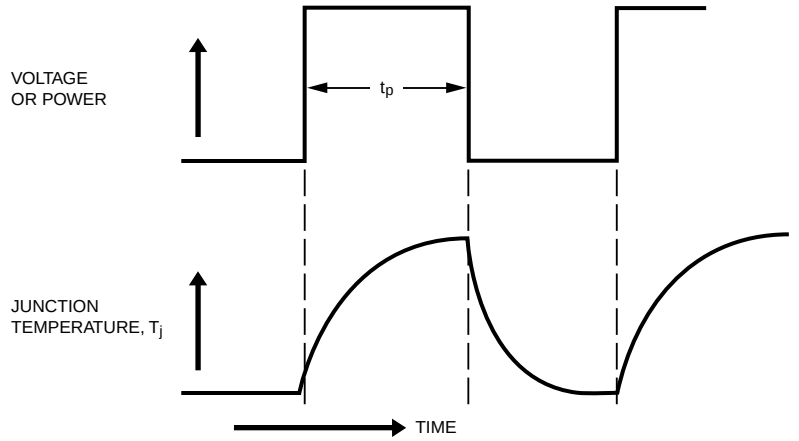
$$\tau = \left[\frac{2F}{\pi}\right]^2\left[\frac{\rho C}{K_{TH}}\right] \qquad (10a)$$

Where:

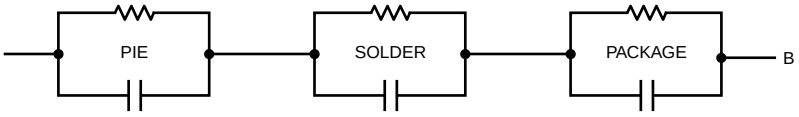
F = die thickness
ρ = density of semiconductor
K_{TH} = thermal conductivity
C = specific heat of semiconductor

The constant $\rho C / K_{TH}$ will be calculated for two semiconductors, silicon and GaAs.

* This is Eq. (9.64a) in reference [1].



(a) JUNCTION TEMPERATURE vs. TIME FOR $\tau < t_p$



(b) TIME CONSTANTS IN CASCADE

Figure 8. Thermal Time Constants

Figure 9. Temperature vs. Distance Across A Large Multi-finger Die

1. Silicon (Si)

Equation 10b:

$$\rho = 2.33\ \text{gr/cc}$$
$$C = 0.7\ \text{J/gr°C} \triangleq 0.7\ \text{W-sec/gr°C}$$
$$K_{TH} \cong 1.00\ \text{W/cm°C}$$
$$\text{Then}\ \frac{\rho C}{K_{TH}} = \frac{2.33 \times 0.7}{1.0} = 1.63\ \text{sec/cm}^2$$

2. Gallium Arsenide (GaAs)

Equation 10c:

$$\rho = 5.31\ \text{gr/cc}$$
$$C = 0.35\ \text{J/gr°C} \triangleq 0.35\ \text{W-sec/gr°C}$$
$$K_{TH} \cong 0.44\ \text{W/cm°C}$$
$$\text{Then}\ \frac{\rho C}{K_{TH}} = \frac{5.31 \times 0.35}{0.44} = 4.22\ \text{sec/cm}^2$$

The following examples of a pulsed *silicon* transistor will show the importance of the thermal time constant.

Let:
θ = 50°C/W
T_A = 25°C
P_D = 5 watts, peak
F = 5 mils = 0.0125 cm

Use the following pulse lengths:
(1) 10 μsec
(2) 100 μsec
(3) C.W.

Calculate τ, the thermal time constant:

$$\tau = \left[\frac{2F}{\pi}\right]^2\left[\frac{\rho C}{K_{TH}}\right] = \left[\frac{2(0.0125)}{\pi}\right]^2 1.63$$
$$= 103\,\mu s = 1.03\times10^{-4}\,sec$$

Then:
a.

$$T_j = 5(50)\left[\frac{4}{\pi^{\frac{3}{2}}}\right]\left[\frac{10^{-5}}{1.03\times10^{-4}}\right]^{1/2} + 25$$
$$= 56 + 25 = 81°C \text{ for a pulse length of } 10\,\mu sec \qquad (10e)$$

Or:
b.

$$T_j = 5(50)\left[\frac{4}{\pi^{\frac{3}{2}}}\right]\left[\frac{10^{-4}}{1.03\times10^{-4}}\right]^{1/2} + 25$$
$$= 202°C \text{ for a pulse length of } 100\,\mu sec \qquad (10f)$$

Or:
c.

$$T_j = 5(50) + 25$$
$$= 275°C \text{ for CW}$$

Note that a Gallium Arsenide device under otherwise the same conditions would have a much higher temperature.

$$\theta = 50\left[\frac{1}{0.44}\right] = 113°C/W$$
$$\tau = 103\left[\frac{4.22}{1.63}\right] = 267\,\mu sec \qquad (10g)$$

1. Therefore, with a 10 μsec pulse:

Equation 10h:

$$T_j = 5(113)\left[\frac{4}{\pi^{\frac{3}{2}}}\right]\left[\frac{10^{-5}}{2.67\times10^{-4}}\right]^{1/2} + 25$$
$$= 103°C$$

2. Or, with a 100 μsec pulse:
T_j = 248°C

3. Or, under CW conditions:

T_j = 113 x 5 + 25 = 590°C

The result above shows that pulses short compared to τ give a very small temperature rise, while the long pulses result in a temperature rise closer to the CW condition. Pulse lengths greater than 2τ result in essentially the CW temperature.

III. Measurement of Thermal Resistance

There are two basic approaches to the measurement of θ, the thermal resistance. A method considered by some to be the most basic uses an infrared scanner to measure the surface temperature by its infrared emission. This system has both advantages and disadvantages.

Infrared Measurement of θ
Advantages:
1. Reads peak, not average, locates "hot spot" temperature to 0.3 mil accuracy.
2. Can give temperature profiles of larger devices.

Disadvantages:
1. High cost.
2. Slow
3. Destructive (uses constant emisivity coating on die)

A temperature profile of a large device will be similar to Figure 9 where the temperature peaks occur at the emitters.

The second method of temperature measurement depends on the temperature dependence of the forward voltage across a diode. This can be emitter-base voltage of a bipolar or the gate-source voltage of an FET.

For a bipolar transistor:

$$I_E = A_e q n_i^2 \frac{D_B}{N_B}\left[\exp\frac{qV_{be}}{kT_j} - 1\right] \qquad (11)$$

Where:
I_E = emitter current
V_{be} = emitter-base voltage
V_j = temperature
A_e = emitter area
n_i, D_B, N_B = material constants

Using the previous example geometry (equation 5a), V_{be} is found to have a slope ≅ 1.6 MV/°C for I_E = 1 mA.

Therefore, by measuring V_{be} the junction temperature can be determined. The temperature thus measured is an *average* and does not indicate the peak temperature as the thermal scan method can.

Measuring temperature by the ΔV_{be} method is very simple. The device to be tested is biased to a constant low "measuring" current; e.g., 1 mA. It is then momentarily pulsed to a higher current (pulse

length >>τ). V_{be} is then measured immediately after the device returns to the lower current condition. The delay should be less than 1% τ. V_{be} is then compared to the low current "cold" value.

$$\theta = \frac{\Delta T}{\Delta P_D} = \frac{\frac{1}{mV/C} \bullet \left(\Delta V_{be}\right)^*}{VI_{Hi} - VI_{meas}} \quad (12a)$$

* in mV

For example, our example geometry is pulsed from 1 mA and 10 volts to 30 mA and 10 volts. V_{be} changes from 0.704 volts (cold) to 0.653 volts (hot). Note that the temperature reduces V_{be}; current increases V_{be}.

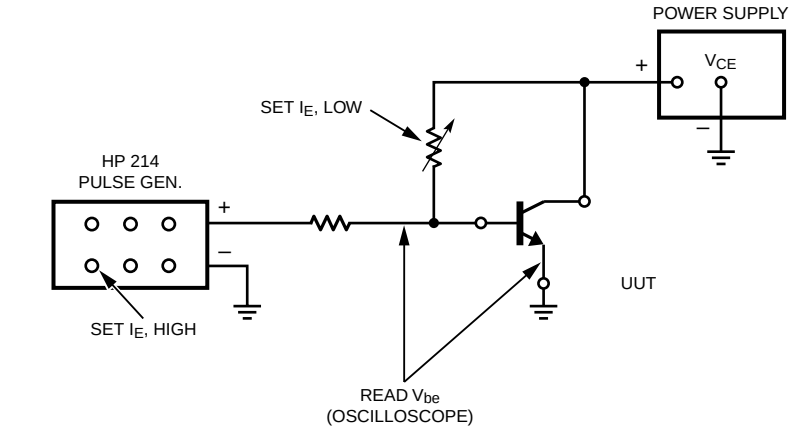
Calculate θ as shown in Equation 12b.

Equation 12b:

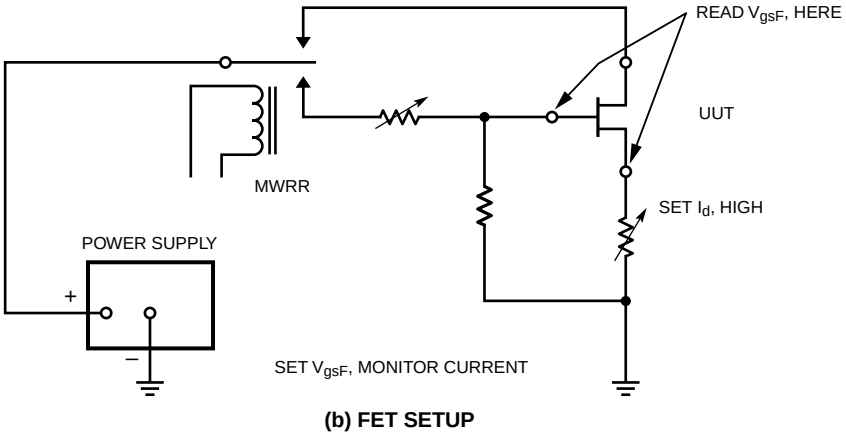
$$\theta = \frac{°C}{mV} \times \frac{\Delta V_{be}}{\Delta P_D} = \frac{1}{1.6} \times \frac{704 - 653}{\left(0.03 - 0.001\right)10} = 110°C/W$$

The instrumentation for the measurement includes a pulse generator, oscilloscope (with Tektronix type W plug-in), and power supply. Figure 10 shows simplified test setups for bipolar and FET transistors. Note that in the case of the FET, the gate bias is negative in the higher power dissipating mode and positive in the measuring mode.

Hewlett-Packard uses a θ_{jc} test set to measure ΔV_{be} semi-automatically on both types of transistors. The test set uses a sample-and-hold circuit to remember V_{be} and displays it on a digital voltmeter. Thus, for special applications, devices can be screened individually for θ_{jc}.



(a) BIPOLAR SETUP



(b) FET SETUP

Figure 10. Simplified Test Setups for Measuring Thermal Resistance of (a) Bipolar Transistors and (b) FETs

IV. General Comments on Thermal Ratings

The thermal resistance may be stated in a number of ways, the most common of which is θ_{jc} , the thermal resistance between the junction and the external case (or package). It includes:

$$\theta_{jc} = \theta_{die} + \theta_{solder} + \theta_{case} \qquad (12c)$$

The free air thermal resistance is much higher since the case is not tied to a sink, but must lose heat by radiation and convection. If heat sinking is provided through the leads only, then θ has a value between θ_{jc} and θ free air.

Derating curves are determined as follows: The maximum dissipation in the case of a bipolar transistor is determined from what is called the “safe operating area.” Within that area the VI product is such that secondary breakdown will not occur. The maximum dissipated power is then computed from this characteristic and would always be less than the maximum voltage times the maximum current. A typical value for P_{Dmax} for a small-signal microwave transistor is 100 – 200 mW.

Figure 11 shows a derating curve. P_{max} is determined from the safe operating area as explained above. The maximum junction temperature is determined from reliability studies and can vary depending upon the MTBF desired. A value of 200°C is typical for silicon bipolar transistors. The breakpoint in the curve is where the junction is at 200°C and the power is P_{max} ; i.e.,

$$T_x = 200 - P_{Dmax}\theta \qquad (12d)$$

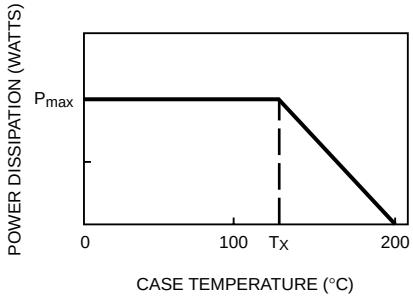


Figure 11. Power Derating Curve

When the temperature of the case is greater than T_x , the dissipation is no longer determined by the safe operating area but is a function of the thermal resistance and the maximum junction temperature.

For microwave FETs, the value for maximum channel temperature is typically between 150°C and 200°C. It will usually correspond to an MTBF on the order of 10^5 hours.

Appendix

A. Summary of Symbols

Symbol	Description	Units
ΔT	temperature rise	°C
P_D	power dissipation	watts
θ	thermal resistance	°C/watt
T_j	junction temperature	°C
T_A	ambient temperature	°C
K_{TH}	thermal conductivity	watts/cm • °C
L	gate length (of the FET)	cm
F	die (chip) thickness	cm
τ	thermal time constant	seconds
t	time	seconds
ρ	density of material	gram/m^3
c	specific heat	watt sec/gram • °C
t_p	pulse width	seconds
I_E	emitter current	amperes
V_{be}	emitter-base voltage	volts
A_e	emitter area	cm^2
n_i	intrinsic carrier density	cm^{-3}
D_B	diffusion constant for minority carriers in the base	cm^2 sec^{-1}
N_B	free carrier density in the base	cm^{-3}

B. References

1. Pritchard, R.L.; *Electrical Characteristics of Transistors*, McGraw-Hill, New York, 1967; Chapter 9.4

2. Linstead, R.D. and Surty, R.J.; "Steady State Junction Temperature of Semiconductor Chips." *IEEE Transactions on Electron Devices*, Vol. ED-19, No.1, Jan. 1972; pp. 41-44.

3. Cohn, S.B.; *IRE Transactions on Microwave Theory and Techniques*, Vol. MTT-2, No. 2, July 1954; pp. 52-57.

4. Oliver, A.A.; *IRE Transactions on Microwave Theory and Techniques*, Vol. MTT-3, March 1955; pp. 134-143.

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